A SINGLE PHASE SERIES ACTIVE POWER FILTER FOR HARMONIC COMPENSATION OF NONLINEAR LOADS

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ABSTRACT

In this paper a method of controlling a single phase series active power filter is proposed. In this method a total harmonic-current signal is detected, directly in real time, as a difference between the load current and its fundamental component. Processing of this signal is used in controlling the switching pattern of a compensating voltage-fed PWM inverter. With this method, load harmonics can be compensated even under frequency excursions of the power system source. Theoretical analysis and computed performance are corroborated by experimental results of a laboratory prototype.

KEYWORDS: Harmonic current compensation, Series active power filter, Single-phase harmonic compensation.

1- INTRODUCTION

The compensation for harmonic generated by power electronic equipment becomes increasingly important as its use in industrial application is increasing. Passive filter have been used for this purpose, however they have the limitations of being subjected to detuning due to variations in the source frequency, impedance and/or filter parameters. They also can be bulky, costly and may fall into series or parallel resonance with the source impedance. Due to these limitations of passive filters, along with the remarkable progress in the speed and capacity of semiconductor switching devices such as GTO thyristors and IGBT's , active filters have been introduced. Their basic principle were proposed in the beginning of the 1970s, since then attention has been paid to active filters [1-9].

Active filter have been classified from system configuration point of view to shunt series, hybrid active and passive, and combination of shunt active and series active filter [10]. They have, also, been classified from power circuits viewpoint to a voltage-fed PWM inverter and a current-fed PWM inverter. Almost all active filters, which have been put into practical applications, have adopted the voltage-fed PWM inverter as the power circuit. This is because the voltage-fed PWM inverter is higher in efficiency and lower in initial costs than the current-fed PWM inverter [9]. The shunt active filter injects a

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compensating current into the supply to cancel current harmonics, however the series active filter injects compensating voltage, that is it has a dual relationship with the shunt active filter [10].

The compensating current or voltage command is decided depending on the control strategy employed. There are mainly two kind of control strategies, one is based on the Fast Fourier Transform (FFT) in the frequency domain [7] and the other is based on the instantaneous active and reactive power theory, or the so-called "p-q theory", in the time domain [11]. In the FFT method, two FFT transformations are needed which take about 80mS to complete [12]. Also, a nonsynchronous sampling error will be caused by a distorted voltage signal. However in the method which is based on the p-q theory sophisticated analogue circuits are adopted to implement real time harmonic detection of distorted current in a three-phase circuit. In addition, it is not applicable to single phase circuits.

This paper is concerned with a single phase series active power filter. Several single phase control algorithms have been developed, but the performance of some still to be improved. The half-cycle integration algorithm has the inherent problem that it produces a large error when the load currents contains even-order harmonics [13]. The current-sampling detection algorithm cannot compensate effectively as the load current is seriously distorted [14]. The performance of these two algorithms will be degraded under distorted mains voltage. An algorithm for power factor and harmonic compensation based on calculation of real part of the fundamental load current, has considered the effect of distorted mains voltage [15]. However, it employs the full-cycle integration algorithm to extract the real part of fundamental load current which is subjected to large compensation error under variations of mains frequency.

In this paper a straightforward approach for controlling an active power filter to improve harmonic compensation accuracy under distorted and/or frequency excursive mains voltage is presented. It is applied to a series active power filter. In this approach a phase locked reference input is processed by an adaptive switched capacitor filter to produce an output which equals the fundamental signal of the distorted current input in amplitude and phase. This output is subtracted from the primary input to cancel its fundamental component, consequently the output will be the sum of all harmonic current signal. The magnitude and sign of this signal are used to control a voltage source PWM inverter. This inverter feeds a current transformer whose primary is connected in series with the mains line. Simulated performance of the proposed approach as applied to a single phase thyristor controller harmonic compensation is verified by experimental results.

2- CONCEPT OF THE PROPOSED METHOD

A controlled voltage source V_c is injected in series with a line feeding a nonlinear load to circulate harmonic currents equal in magnitude and opposite

in phase to that originally generated by the load. This V_c is obtained across the primary of a current transformer CT whose secondary is fed from a controlled voltage source PWM inverter as shown in Fig. 1. The switching instant of the

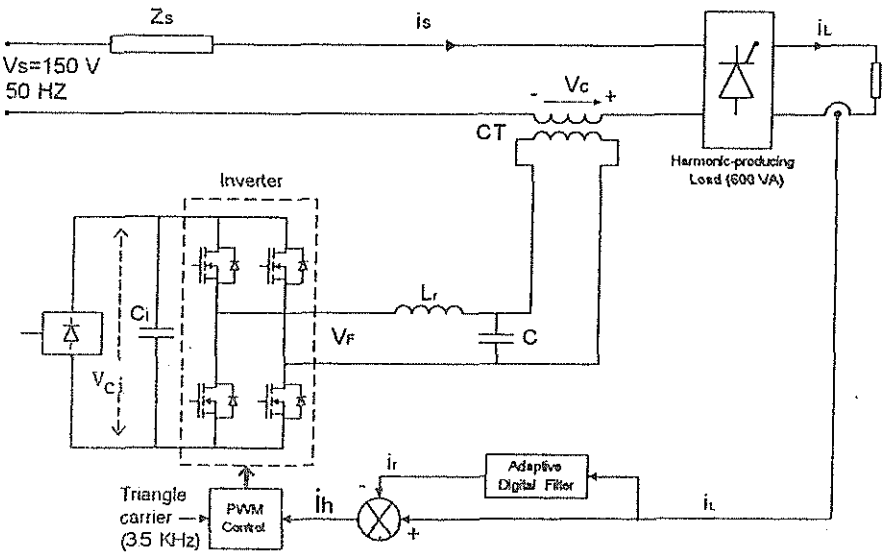


Fig. 1 **Circuit configuration of the power and control systems.**

inverter is controlled by the polarity and magnitude of the total harmonic current signal $i_h(t)$ in conjunction with a PWM control. This $i_h(t)$ can be obtained considering, generally, a nonlinear load current signal $i_L(t)$ represented as,

$$i_L(t) = \sum_{n=1}^{\infty} I_n \sin(n\omega t + \theta_n) \qquad (1)$$

where: I_n and θ_n represent the amplitude and the phase of the nth -order harmonic load current without the active filter being in action. This current can be subdivided into fundamental and harmonic components as,

$$i_L(t) = I_1 \sin\omega t + \sum_{n=2}^{\infty} I_n \sin(n\omega t + \theta_n) \qquad (2)$$

where I_1 is the peak value of the fundamental current signal. A reference signal $i_r(t)$, equal in magnitude and phase to the fundamental current signal, can be generated, using an adaptive bandpass digital filter, which can be represented by,

$$i_r(t) = I_1 \sin\omega t \qquad (3)$$

The total harmonic current signal $i_h(t)$ can be obtained by subtracting $i_r(t)$ signal from $i_L(t)$ signal as shown in Fig. 2 which yields,

$$i_h(t) = i_L(t) - i_r(t) \qquad (4)$$

This $i_h(t)$ is amplified by a gain G and is inputted to the PWM controller as a voltage reference. This reference is compared with a triangle-wave carrier to produce the switching pattern.

A harmonic equivalent circuit of the proposed system is shown in Fig. 3. It is assumed that the active filter is represented by a controllable harmonic voltage source V_c and Z_s is the source impedance. The nonlinear load can be generally

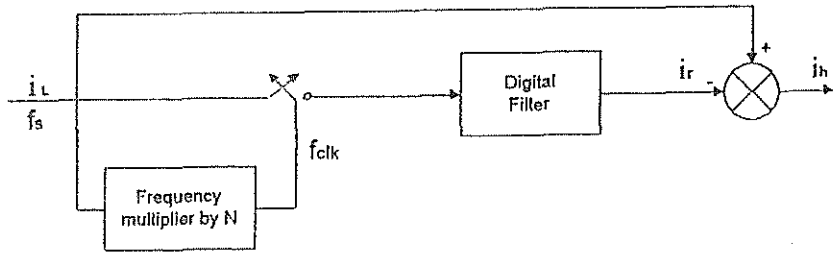


Fig. 2 **Block diagram of harmonic current detector.**

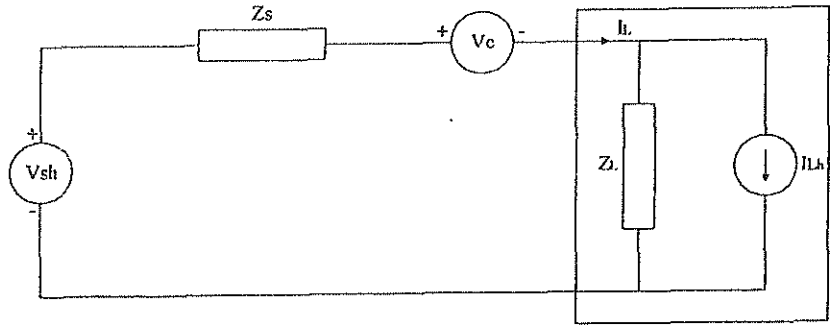


Fig. 3 **Harmonic equivelant circuit of the proposed system.**

represented as given in reference [16] by an effective complex impedance Z_L in parallel with a harmonic current source I_{Lh}. The residual load harmonic current I_{rLh} after compensation can be determined by superposition as,

$$I_{rLh} = \frac{V_{sh} - V_c}{Z_s + Z_L} + I_{Lh} \qquad (5)$$

If the source voltage V_s is sinusoidal i.e V_{sh}=0, Then,

$$I_{rLh} = I_{Lh} - V_c / (Z_s + Z_L) \qquad (6)$$

Ideally I_{rLh} should be equal to zero i.e,

$$I_{Lh} = V_c / (Z_s + Z_L) \qquad (7)$$

Description of the control and power circuit of the prototype which is used to examine the proposed controlling approach is given in the subsequent sections.

3- POWER CIRCUIT

Representation of the power circuit of the prototype is as shown in Fig. 1. In which a PWM inverter is inserted in series with the mains or load through a current transformer CT. A capacitor C_i is connected across the dc side of the PWM inverter. The capacitor voltage V_{ci} is kept constant at 15Volts by

connecting a diode rectifier on the dc side. The energy corresponding to the switching and conducting losses in the inverter is supplied from this rectifier. An L-C passive filter is connected at the output of the PWM inverter to suppress switching ripples of voltage and currents generated by the inverter. The filtering characteristics of this passive filter is substantially affected by the series combination of the source and load impedances. The effect of these impedances will be more pronounced for low ratio CT and low switching frequency. The practical range of the switching frequency is usually low 2-3 KHz [8]. Design of this L-C filter considering the load and source impedances is as given below.

3. 1 Design of the L-C Passive Filter

The equivalent circuit seen from the PWM inverter can be represented as shown in Figs. 4a & b. Z_{eq} is the sum of Z_S, Z_L, and Z_{ct} which are seen from the secondary of the CT and can be expressed as,

$$Z_{eq} = (\frac{n_s}{n_p})^2 (Z_s + Z_L + Z_{ctp}) + Z_{cts} \qquad (8)$$

where Z_{ctp} , and Z_{cts} are primary and secondary coil impedances,

$\frac{n_s}{n_p}$ CT turns ratio.

The total impedance Z_T seen by the inverter output voltage V_F, shown in Fig. 4b, can be written as,

$$Z_T = Z_r + Z_c Z_{eq} / (Z_c + Z_{eq}) \qquad (9)$$

The harmonic current $I_{Fe}(n)$ flows through Z_{eq} can be expressed in terms of the ripple voltage $V_F(n)$ as,

$$I_{Fe}(n) = V_F(n) Y(n) \qquad (10)$$

where $1 / Y(n) = Z_T(n)(Z_c(n) + Z_{eq}(n)) / Z_c(n) \qquad (11)$

The impedance given by Eq. (11) should be low for all the range of harmonic frequencies to be compensated for. However, it should be high beyond this range to attenuate the ripple frequencies which are produced due to switching of the PWM.

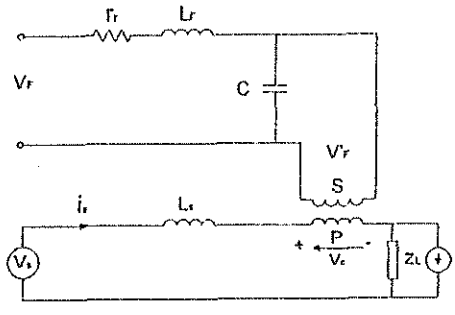


Fig. 4a **Equivalent circuit seen from the PWM inverter**

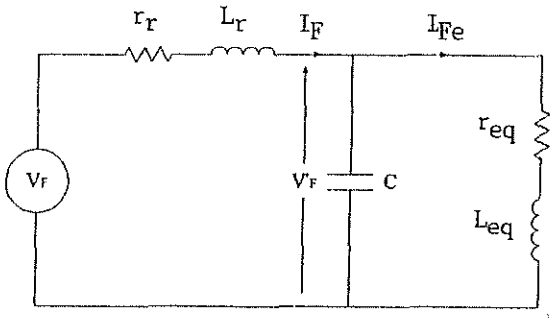


Fig. 4b **Equivalent circuit seen from the PWM inverter referred to the secondary side of CT.**

The resonance frequency ω_r terminating this range, can be obtained in terms of the system and filter parameters substituting from Eqs. (8) and (9) into (11) and equating the imaginary part to zero yields,

$$\omega_r = \sqrt{\frac{L_{eq} + L_r}{L_{eq}\, L_r\, C}} \qquad (12)$$

This resonance frequency must lie between an upper limit which is the switching frequency and a lower limit equals to the highest harmonic frequency to be compensated. An accurate value of ω_r can be determined which provide the minimum total harmonic distortion. The percentage total harmonic distortion (THD) can be written as,

$$THD\% = \frac{100}{I_1}\sqrt{\sum_{n=2}^{\infty}\left(I_{Lh}(n) - (n_s/n_p)I_{Fe}(n)\right)^2} \qquad (13)$$

where $I_{Lh}(n)$ and $I_{Fe}(n)$ are the RMS of the harmonic current produced by the load and active filter respectively.

I_{Fe} is given by Eq. (10), $I_{Lh}(n)$ is obtained from Eq. (15) which is given for the specified R-L load fed by a thyristor controller. For a given value of C, Eq. (12) is solved for L_r. Substitute with this value of L_r into Eqs. (11) and (10) to obtain $I_{Fe}(n)$. Then substitute in Eq. (13) to calculate the THD for the specified load current. These calculations are repeated for different values of ω_r. The results of calculations reveals the value of ω_r at which the minimum THD occurs as is shown in Fig. 4c. This value of ω_r is 2 π(600) *rad / Sec* is considered for the L-C filter design which yielded C= 6μF and L_r=1.2mH. The corresponding frequency response plot of 1/Y is shown in Fig. 4d.

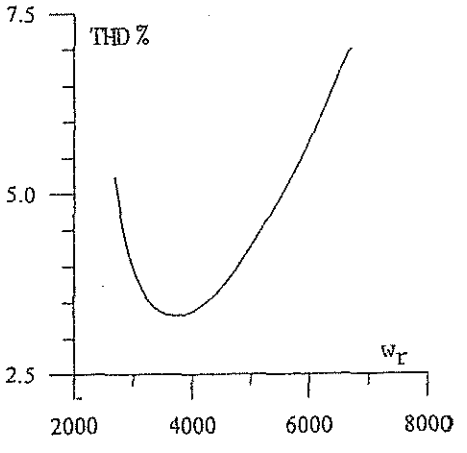


Fig. 4c **Variation of THD of load current versus ω_r after compensation.**

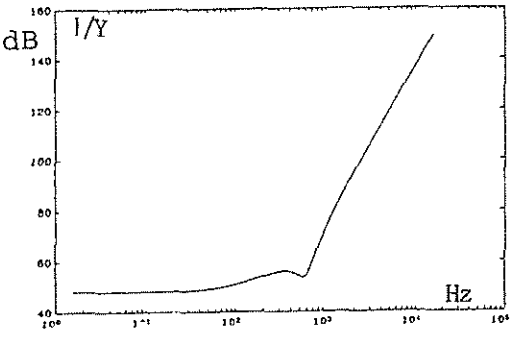


Fig. 4d **Frequency response of 1/Y(n) at minimum THD of load current.**

4- CONTROL CIRCUIT

The control circuit is made up of two parts. The first is concerned with the detection of harmonic signal $i_h(t)$ which requires the fundamental frequency signal to be detected and subtracted from the total current signal $i_L(t)$. The second is concerned with the PWM and steering circuits. These are described in the two subsequent sections.

4.1 Harmonic Signal Detector

A circuit diagram of the harmonic signal $i_h(t)$ detector is shown in Fig. 5. In this figure, the input current signal $i_L(t)$ is fed to the fundamental frequency component detector and to the noninverted terminal of a differential amplifier A_1. The output $i_1(t)$ of the fundamental component detector is fed to the

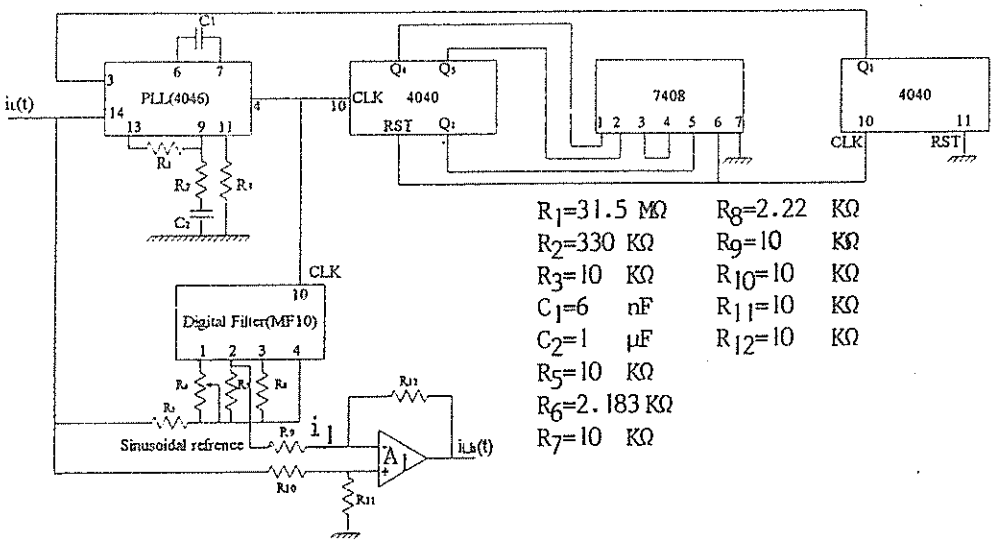


Fig. 5 **Circuit diagram of harmonic current signal detector.**

inverted terminal of A_1. Since $i_1(t)$ is a pure sinusoidal, the output $i_h(t)$ will be composed of the sum of all harmonic components exist in the $i_L(t)$.

The fundamental component detector is a bandpass second order digital (Sampled data) filter of the type MF10. The center frequency of which is being locked to the supply fundamental frequency f_S. This locking is achieved by making the ratio of the clock frequency f_{CLK} of the MF10 to the input signal frequency f_S to be always constant. This is realised by obtaining the f_{CLK} from a phase locked loop PLL. The employed PLL consists of a digital phase detector and a voltage controlled oscillator fabricated in an integrated circuit chip 4040 CMOS, a low pass filter and a divide by N of 100 binary-counter (two cascaded 4040). The PLL is set to provide the MF10 with $f_{CLK} = Nf_S$ of 5KHz. Determination of the value of the parameters, shown in Fig. 4, C_1, C_2, R_1, R_2 and R_3 of the PLL and R_5, R_6, R_7 and R_8 of the MF10 is based on the approach of tuning and locking of the MF10 reported in reference [17].

Combination of the MF10 with the PLL in the described way, makes the MF10 works as an adaptive bandpass digital filter. The filtering characteristics of which will be fixed regardless of f_S variations. This can be explained with reference to Fig. 6. If f_S was varied from 50 to 100Hz with f_{CLK} had been kept constant at 5KHz the attenuation characteristics would have been changed from curve a to that given by curve b and the corresponding phase curves changed from d to e. It can be seen that at, for example, the second harmonic corresponding to both cases (i.e 100 and 200Hz) the attenuations would vary from -34 to -48dB and the phase angle vary from -2.8 to 3.1 rad. In order to have the same characteristics (-34dB, -2.8rad), the filter must be redesigned at the new center frequency (100Hz). However if f_{CLK} was varied from 5 to 10 KHz corresponding to variation of f_S from 50 to 100Hz, as in the case with the proposed adaptive bandpass filter, the characteristics would be as shown by curves c and f. In these curves filter parameters and hence the filtering

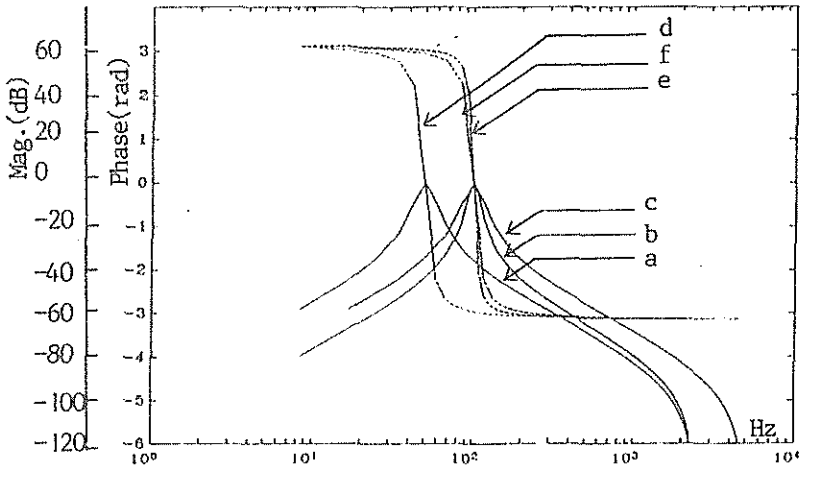


Fig. 6 **Frequency response of the bandpass digital filter:**
- conventional filter (a to b), - adaptive filter (a to c).

characteristics, at the new adopted center frequency (f_0=100), will not be changed from the case of curve a. Where the attenuation and phase are -34dB and -2.8 rad respectively for the second harmonic of both cases. This signifies an adaptive filtering characteristics which is essential in detecting the fundamental frequency signal under distorted and frequency excursive input current signal.

4.2 PWM and Steering Circuit

In Fig. 7, the signal $i_h(t)$ is compared with a triangular carrier wave of 3.5 KHz (fixed frequency). Using an op. amp comparator A_2. The output of A_2 which is a PWM signal is made available at the input of And gates G_1 and G_2. The positive and negative polarities of $i_h(t)$ are detected by A_4 and A_3

respectively. If $i_h(t)$ is positive G_1 will be enabled and releases the PWM signal to be amplified through pulse amplifier, fed via an optocoupler from a darlington transistor array inverter ULN2003A, in order to trigger both transistors T_1 and T_4 of the power inverter. However, if $i_h(t)$ is negative G_2 will be enabled and releases the PWM signal to trigger transistors T_2 and T_3. Output of the inverter is injected to the load circuit and is effectively subtracted from the originally existed harmonics. The level of harmonic compensation achieved can be assessed via system simulation.

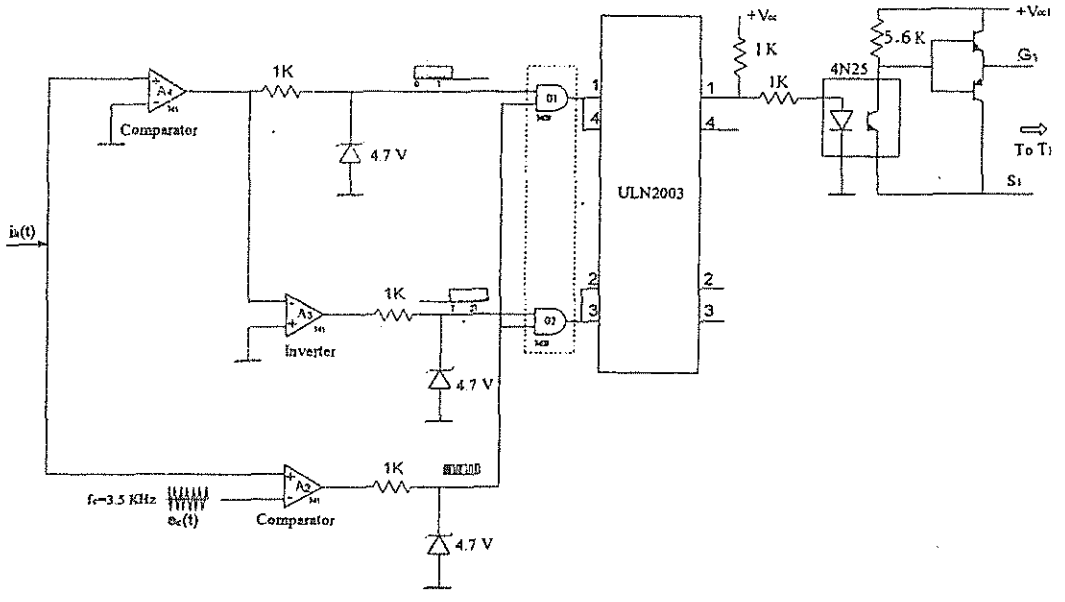


Fig. 7 **PWM and steering circuit.**

5- SYSTEM SIMULATION

5.1 Load Simulation

An R-L load of R= 60Ω and L= 64mH fed from a source of 150V, 50Hz and inductance Ls= 0.023mH, through a full wave thyristor controller is considered. The firing angle α of the controller was set to 33°. The corresponding load current can be determined, up to the 9th harmonic component, by Fourier series as,

$$i_L(t) = 3.548\sin(\omega t - 18.85°) + 0.2908\sin(3\omega t - 11.25°) + 0.198\sin(5\omega t - 70.8°) + 0.125\sin(7\omega t - 127.5°) + 0.0743\sin(9\omega t - 5.5°) \quad (14)$$

The thyristor controller together with the R-L load can be represented, for a sinusoidal source voltage, based on the method reported in reference [16], by an impedance $Z_L = 59.92 + j2\pi f * 0.064\Omega$ in parallel with a current source i_{Lh}, where,

$$i_{Lh}(t) = 0.2908\sin(3\omega t - 11.25°) + 0.198\sin(5\omega t - 70.89°)$$
$$+0.125\sin(7\omega t - 127.5°) + 0.0743\sin(9\omega t - 5.5°) \qquad (15)$$

5.2 Control System Simulation

The triangular carrier wave $e_C(t)$ of the PWM can be expressed by Fourier analysis as,

$$e_C(t) = \frac{8E_C}{\pi^2} \sum_{n=1,3,5,..}^{\infty} \frac{1}{n^2}(-1)^{\frac{(n-1)}{2}} \sin n\omega_C t \qquad (16)$$

where E_C is the peak value of the triaugular wave and ω_C is its angular frequency. The signal $i_h(t)$ is given by the harmonic terms of Eq. (14) scaled by transducer constant K and harmonic detector gain G, to yield the modulating signal. The maximum value E_S of this modulating signal is adjusted, via the loop gain, to be equal to E_C. That is to have a modulation degree $M = E_S/E_C = 1$. Comparing $e_C(t)$ with $i_h(t)$ yields the switching pattern and inverter output $v_F(t)$ as,

$$\begin{aligned} v_F(t) &= +V_{Ci} && for && e_C(t) < i_h(t) > 0 \\ &= 0 && for && e_C(t) > i_h(t) > 0 \\ &= -V_{Ci} && for && e_C(t) > i_h(t) < 0 \\ &= 0 && for && e_C(t) < i_h(t) < 0 \end{aligned} \qquad (17)$$

Generally, $v_F(t)$ will be a nonperiodic PWM function. It is injected into the combination of the passive L-C filter in parallel with equivalent impedance of the system and load as shown by the equivalent circuit of Fig. 4b. The equations describing the action of the active filter with the system and load can be written in the state space form as,

$$\frac{d}{dt}\begin{bmatrix} i_F \\ i_{Fe} \\ v'_F \end{bmatrix} = \begin{bmatrix} -r_r/L_r & 0 & 1/L_r \\ 0 & -r_{eq}/L_{eq} & 1/L_{eq} \\ 1/C & -1/C & 0 \end{bmatrix}\begin{bmatrix} i_F \\ i_{Fe} \\ v'_F \end{bmatrix} + \begin{bmatrix} 1/L_r \\ 0 \\ 0 \end{bmatrix} v_F \qquad (18)$$

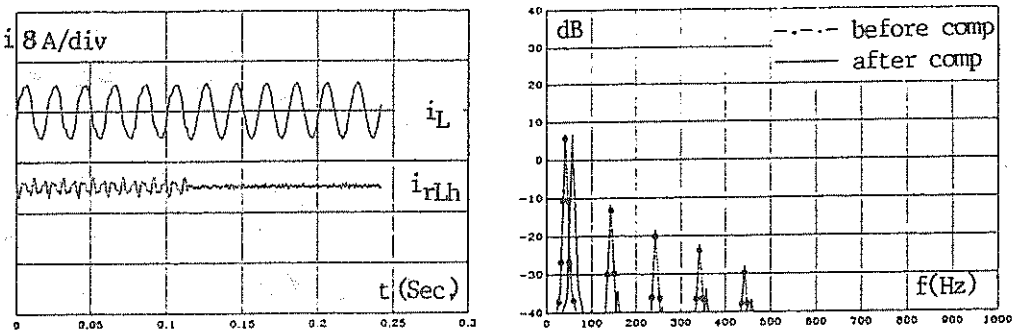
where $i_{Fe}(t) = \frac{n_p}{n_s} i_{Fh}(t)$, $r_r = 3.5\Omega$, $L_r = 0.012$H, $r_{eq} = 241.8\Omega$, $L_{eq} = 0.396$H, and $C = 6\mu$F.

In order to account for the inclusion of supply frequency variations, the term ωt in Eq. (14) is replaced by $\omega(t - t_0) + 0.5r(t - t_0)^2$. Where t_0 is the instant on wave at which frequency start to increase, and r is the rate of change of the angular frequency in rad/Sec^2.

6-RESULTS

Equations (17), and (18) were solved for $i_{fe}(t)$ using Runge Kutta routine. The values of the parameters adopted were those used for the experimental prototype, which are listed in the Appendix. At each sample $i_{fh}(t)$ was obtained

and subtracted from $i_L(t)$. The resulted current $i_{rLh}(t)$ is plotted as shown in Fig.8-a before and after compensation. The corresponding frequency spectrum is shown in Fig. 8-b. It can be observed from these figures that there is a substantial effect of the series active filter in reducing the contents of the line

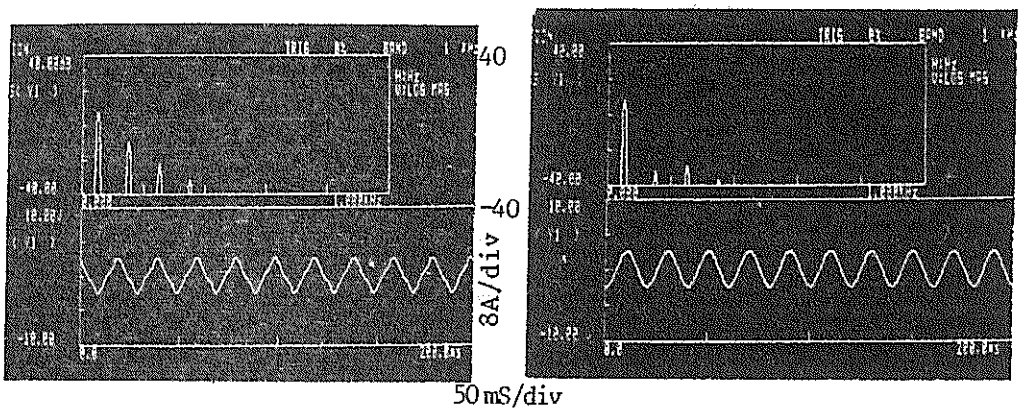


(a) (b)

Fig. 8 **Simulation results before and after compensation:**
a- current waveforms, b- frequency spectrum of load current.

current harmonics produced by load. This result has been confirmed by the results obtained experimentally from the prototype as shown by the wave analyser traces of Figs. 9a, and b.

The response of the active filter for supply frequency variations was examined by imposing a rate of increase in the angular frequency by $650 rad/Sec^2$, in the supply current frequency. The result is shown in



(a) (b)

Fig. 9 **Frequency spectrum and load current waveform:**
a- before compensation b- after compensation.

Fig.10, the frequency is increased from 50 to 62Hz in 0.225S, in which the capability of the proposed controlling method to compensate the load harmonics under frequency variation is therefore illustrated.

The transient response of the prototype was examined experimentally by the application of a sudden increase of about 100% in load current. The result is shown by the oscilloscope traces of Fig. 11. This shows the capability of the

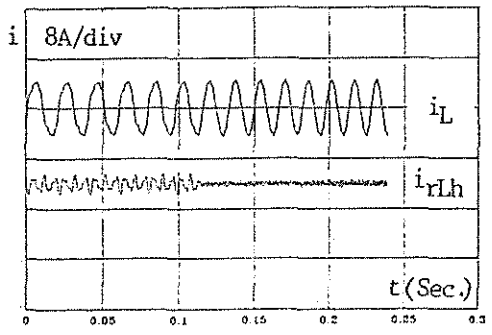


Fig. 10 **Current waveforms before and after compensation for frequency increase from 50 to 62Hz in 0.225 S (650 rad/Sec^2).**

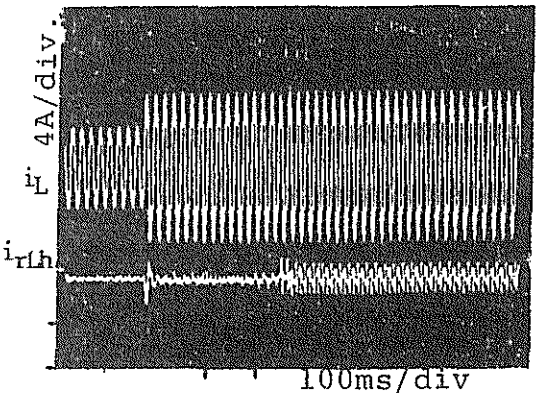


Fig. 11 **Current waveforms with and without compensation for sudden increase of the load current of about 100%.**

proposed controlling method in providing a full harmonic compensation within one cycle time. This response time is regarded as an improvement, as far as single phase active filters are concerned over other algorithms which have been reported [15].

7. CONCLUSIONS

A straightforward method for controlling a single phase series active power filter for load current harmonic compensation has been presented. In this method, total harmonic current signal has been detected by canceling the fundamental frequency component using an integrated circuit band-pass switched capacitor filter. The center frequency of this filter has been locked to supply frequency via a phase locked loop. The detector has performed effectively as an auto adaptive notch filter. The switching ripple passive L-C filter parameters has been correlated with the system and load impedances based on minimizing the net harmonic current distortion. The presented approach can be applied to any active filter, series or parallel with distorted and/or frequency excursive supply voltage. Simulation results and experimental tests conducted on a prototype validate the principle of the proposed approach. An *important application of proposed controlling technique using only a single phase series* active power filter will be in canceling the common mode frequencies (zero sequence currents) from the 3-phase lines by feeding the PWM with the sum of the 3-phase line currents.

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Appendix

Values of the parameters used for the simulation and experimental prototype are as given below:

- Switching ripple passive filter : capacitor C= 6μF, inductance L_r= 0.012H and resistance r_r= 3.5Ω.
- CT : turns ratio = 2 , primary coil inductance L_{ctp}= 0.014H and resistance r_{ctp}= 0.6Ω. secondary coil inductance L_{cts}= 0.007H and resistance r_{cts}= 0.3Ω.
- Source inductance L_s= 0.01194H.
- PWM inverter : MOSFETs T_1 to T_4 are IRF531 of rating 800VA.
- Capacitor C_i =2200 μF.
- Diode rectifier bridge of rating 100VA.

مرشح قدرة فعال أحادى الوجه توالى لتعويض توافقيات الأحمال اللاخطية

تعتبر مشكلة وجود التوافقيات فى انظمة القدرة الكهربية قديمة قدم إستخدام التيار الكهربى المتردد. ومن أهم مصادر توليد هذه التوافقيات حاليا هى دوائر القدرة الالكترونية التى تحتوى على أشباه الموصلات.

يقدم هذا البحث طريقة مباشرة للتحكم فى مرشح فعال أحادى الوجه توالى لتعويض توافقيات التيار لحمل كهربى لا خطى ومغذى من مصدر جهد يتعرض لتغيرات كبيرة فى تردده. فى هذه الطريقة يتم الحصول على إشارة تيار التوافقيات الكلية عن طريق إلغاء مركبة التيار الأساسية من إشارة تيار الحمل بإستخدام مرشح دوائر مجمعة رقمى ذو حيز تردد محدد وذو توقيت نبضى قابل للضبط. ويتم التزامن بين تردد منتصف الحيز الترددى وتردد منبع القدرة أوتوماتيكيا عن طريق دائرة مسار تزامنى (PLL) مرتبطة بتردد المنبع . وتقوم هذه الدائرة بتزويد المرشح بنبضات ذات تردد مضاعف بمقدار ثابت من تردد المنبع.

وقد تم أيضا إيجاد الدائرة المكافئة لدائرة القدرة فى المرشح الفعال المقترح مع دائرة حمل لاخطى ودراسة كيفية إتمام عملية تعويض التوافقيات لهذا الحمل. كذلك تم تمثيل المرشح الفعال مع دائرة الحمل ببرنامج على الحاسب الآلى لدراسة إستجابة طريقة التحكم المقترحة لملاشاة التوافقيات فى دائرة الحمل. وقد تم إستخدام هذا البرنامج لتصميم قيم المعاملات المختلفة للمرشح الفعال بحيث تقلل التشوه الكلى لتوافقيات تيار الحمل (THD) ليصل إلى ٣٪.

وقد تم تصميم نموذج معملى للمرشح الفعال المقترح بإستخدام مرشح دوائر مجمعة رقمى من الرتبة الثانية ودائرة مسار تزامنى (PLL)، من نوع مبين الوجه (PD)، للتحكم فى عاكس تعديل عرض النبضة (PWM inverter) ، يستخدم فى تشغيلة اشارة مرجعية مثلثة ، مغذى بمصدر جهد مستمر ويتصل خرج هذا العاكس بدائرة الحمل من خلال محول تيار. وقد تم اختبار هذا النظام معمليا مع حمل حثى (R-L) مغذى من متحكم جهد متردد احادى الوجه.

وقد أظهرت النتائج قدرة المرشح الفعال المقترح على إستقرار التشغيل وتقليل التشوة الكلى للتوافقيات (THD) الناشئة عن وجود متحكم الجهد فى دائرة الحمل من ١٨٪ إلى ٣٪ بالإضافة إلى الملاحقة السريعة لتغيرات تردد المنبع التى تصل إلى حوالى ٧٠٠ درجة زاوية / ثانية[٢].

كما أظهرت النتائج أيضا إمكانية إستخدام الطريقة المقترحه لمرشح فعال لتعويض توافقيات التيار أو الجهد لأنظمة أحادية أو ثلاثية الاوجه سواءً كان هذا المرشح توالى أو توازى.