MENOUFIYA UNIVERSITY
FACULTY OF ENGINEERING
ENG. RESEARCH BULL.
Vol. 17 Part I, 199

PP. 245 : 260
Received at : 5 / 4 / 1994
Accepted at : 19 / 4 / 1994

A LOW POWER TRANSFORMERLESS SINUSOIDAL OR DC OUTPUT VOLTAGE UPS

M.I. MAHMOUD

Faculty of Electronic Engineering-Menouf
Menoufia University
23952 - Menouf - EGYPT

ABSTRACT

A new design approach has been applied to a low power transformerless sinusoidal or DC output voltage uninterruptable power supply (UPS). Theoretical studies and practical implementation have been made for a resonance circuit operated at its no load resonance frequency to obtain a constant sinusoidal current through its load impedance. The resonance tank can be derived through an inverter either by a square wave voltage at the power network frequency or by a sinusoidal distributed pulse width modulated (PWM) voltage at high frequency. The power network frequency technique is used to minimize the power electronic components and the PWM technique is used to minimize the resonance tank size. Theoretical investigations, practical implementations and experimental work illustrate the limitations of the circuit design in each case of sinusoidal or DC output voltage. Duality characteristic of the parallel loaded resonance circuit is studied to achieve many design flexibility. A special computer aided design program for the UPS simulation has been carried out on the previous techniques to determine the construction and the suitable dimensions of the UPS elements in each case study of sinusoidal or DC output voltage. The transient response of the system has been experimentally obtained to identify the real system transfer function at different loading conditions. The control strategy and the controller construction have been designed to provide a good UPS performance. The theoretical and simulation results are validated by the experimental work.

INTRODUCTION

Recently the domain of uninterruptable power supplies (UPS's), becomes a very attractive domain of research. Many attempts [1 - 3] have been considered to realize UPS. The main target of those papers was the improvement of the switching performance of power electronic switches. When the resonance circuits are used, the switching performance may easily be improved. The high frequency is also used to transfer the energy through a transformer without saturating its core. These types of UPS's use the transformation ratio to step up the voltage. Therefore, the transformer is necessary to the UPS operation.

The demand of small size and small power for the UPS's has also recently increased especially in the microcomputer and its applications domain. Low cost UPS's are made to deliver a square wave voltage through a transformer at the power network frequency. Many applications need a sinusoidal or DC operating voltage instead of the square wave voltage of the low cost UPS's. The aim of this work is the investigation of a new design to achieve the agreement between the applications need and low cost UPS. The UPS cost can be divided into two parts, one part is the transformer cost and the other is the cost of power switches and their control circuits. The square wave voltage UPS uses low cost power switch transistors and simple electronics to control these transistors. To minimize the cost of the UPS and obtain an output sinusoidal voltage at the same time, a transformerless UPS has been suggested, analyzed and realized. In this case, the output voltage of the transformerless UPS is a sinusoidal one even when low cost power transistors and their simple control circuits are used. The step up voltage function of a transformer can be obtained and easily changed by means of an inverter and a parallel loaded resonance circuit operating in the constant current mode. The voltage transformation ratio can be easily changed by means of the inverter duty cycle to maintain the output voltage constant as an inverse function of the UPS load impedance. Also, many attempt have been made during this work to reduce the size, weight and cost of the UPS resonance tank. The high frequency PWM techniques are used to show its applicability to this type of UPS in DC or sinusoidal output voltage.

This paper deals with the analysis, practical implementation and experimental verifications of a transformerless sinusoidal or DC output voltage UPS. Theoretical studies have been made for a resonance circuit operated at its no load resonance frequency to obtain a constant sinusoidal current through the load impedance. This circuit is derived by means of a constant square wave voltage delivered by a transistorized inverter at the power network frequency. The constant current level can be varied as a function of the square wave duty cycle to obtain a constant voltage at the load impedance terminals. Computer aided design using a special simulation program has been carried out to determine the construction of UPS and the suitable dimensions of its elements. The transient response of the real system has been experimentally investigated to identify the global system transfer function at different loading conditions. The control strategy and the controller construction have been designed to provide a good UPS performance.

UPS POWER CIRCUIT CONSTRUCTION

Theoretical bases

The main concept in this investigation is to use the behavior of the parallel loaded series resonance circuit operating in the constant current mode [4]. Operation of this circuit at its no load resonance frequency delivers a constant sinusoidal current through the load impedance. Performance, design parameters and some applications of this circuit can be found elsewhere [4 and 5]. The circuit has a disadvantage of parallel resonance phenomena between the load inductive reactance and the output capacitor at certain loading conditions. In this investigation the circuit duality is proposed, verified and its application is suggested to eliminate the parallel resonance phenomena problem. Figure 1 (a) illustrates the parallel loaded resonance circuit while the suggested dual one is shown in Fig. 1 (b). Application of the same circuit analysis and operating conditions on these two circuits show that constant current mode can be equally obtained from each one.

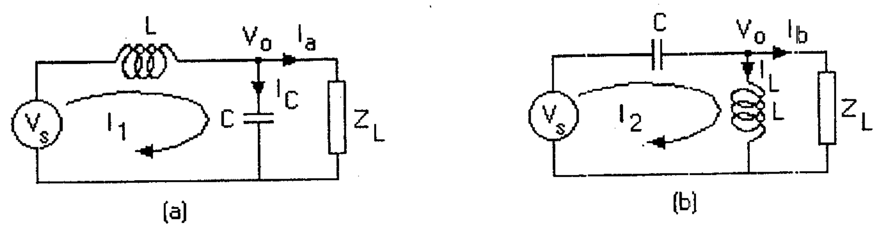

Fig. 1 The duality principals applied to the used resonance circuit.

In the case of sinusoidal input voltage, V_i has the same circuit no load resonance frequency F_0, the constant load current through the load impedance Z_L is:

$$I_a = V_i / j \omega L \quad \text{(Fig. 1(a))} \qquad (1)$$

or

$$I_b = j V_i \omega C \quad \text{(Fig. 1(b))} \qquad (2)$$

The parallel resonance phenomena problem mentioned above may be eliminated when the circuit of Fig. 1(a) is used with inductive load impedance and that of Fig. 1(b) used with capacitive load impedance.

Equations (1) and (2) can be applied to a resonance tank operated through an inverter when one replaces V_i by the effective value of the fundamental component of the inverter output voltage. The resistive part of the resonance tank components is practically small enough to obtain a high Q-factor which in turn filters the frequencies higher than the fundamental one.

Practical implementation

An experimental setup of 250 VA UPS's is constructed to verify the theoretical and simulation results. This prototype is built-up for many UPS configurations, control strategy and theoretical verifications. Figure 2 shows the UPS experimental setup circuit diagram. The UPS power circuit consists of four power switch modules each one is a power switch MOS-FET type with an integrated Zener diode. In most of practical applications, the load power factor is lagging. According to the duality rule mentioned above, the resonance circuit in this case study is parallel loaded at the inductor terminals as shown in Fig. 1(b). The resonance tank is made to resonate at the normal UPS operating frequency. The operating frequency is mainly 50 Hz but the transistors base derive circuits are made to operate at higher chopping frequency (20 kHz) to accept the high frequency PWM in certain case study. The power switch transistors base derive circuits are equipped by an over voltage protection circuit. This circuit reduces the output high voltage produced due to the operation at resonance frequency of the power circuit by reducing the inverter duty cycle. This phenomenon can take place at no load, suddenly disconnected load or light loading conditions. This UPS type is characterized by a constant output current at any load condition including the output terminals short circuit condition. There is no need to protect the UPS power circuit against the over current or terminals short circuiting. To control and keep the output voltage constant, a feedback loop must be realized to compare the output voltage with the input reference. The output voltage is measured and electrically isolated by an optocupler isolator. The feedback signal is rectified through a high precision rectifier, filtered and smoothed by an RC network. The error signal is corrected by a PID controller to achieve a high performance output variables. This corrected error signal acts on the duty cycle of the output of a constant frequency symmetrical square wave generator, in the case of the most economical UPS, to keep the UPS output voltage at its desired value. In the case of high performance UPS, the corrected error signal acts on the amplitude of the output of a constant frequency sine wave generator.

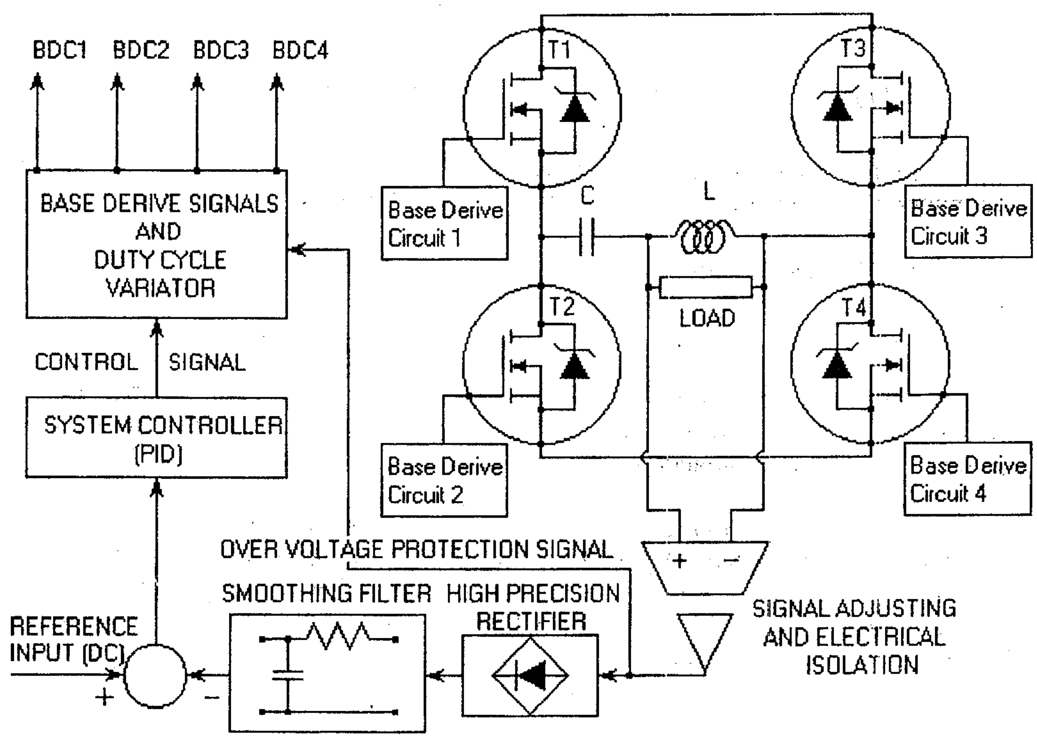

Fig. 2 Experimental setup circuit diagram of the suggested UPS's.

The UPS experimental setup circuit diagram of Fig. 2 is not the most suitable one in all UPS configurations specially for those which are made for minimum cost. A half bridge inverter can be used to reduce the cost and complexity of the UPS power circuit. Although it is appear to be a suitable solution from the component count point of view, the inverters power switch transistors current capability must be doubled with respect to the full bridge inverter. As a result, the overall efficiency of the UPS is reduced and the cost in some cases may be increased. Therefore, a full bridge inverter will be used in this work for the purpose of investigation only.

SIMULATION PRINCIPLES

The discrete analog simulation method [6] is convenience applicable to linear or nonlinear control systems. In this method, a discrete system is synthesized to replace the analogous system so that its signal flow is the same as the original continuous system signal flow. This property of the simulation method makes it a powerful one. The simulation designer, using this method, needs to be familiar only with the original system signal flow. Each block G(s) of a continuous control system is replaced by a sampler S_1, suitable hold type H(s), compensator C(s), the block itself G(s) and a second sampler S_2 to construct the equivalent discrete part as illustrated in Fig. 3.

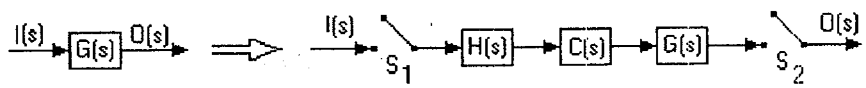

Fig. 3 The construction of the discrete analog system

The circuit shown in Fig. 1(a) can be represented by a block diagram as illustrated in Fig. 4. The numerical recurrent relations of this block diagram using sampling period T can be deduced as:

$$V_L(n) = V_S(n) - V_o(n) \tag{3}$$

where n represents the instant at which the recurrent relations is applied. Using zero order hold and e^{sT} compensator, one obtains:

$$I_1(n) = I_1(n-1) + [T/L]\, V_L(n) \tag{4}$$
$$I_C(n) = I_1(n) - I_a(n) \tag{5}$$

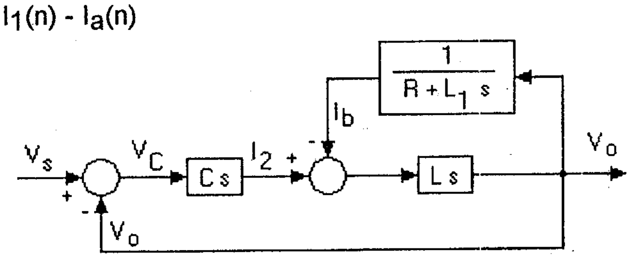

Fig. 4 The block diagram representation of the circuit in Fig. 1(a).

$$V_o(n) = V_o(n-1) + [T/C]\, I_C(n) \tag{6}$$

Using zero order hold without compensator, one obtains:

$$I_a(n) = e^{-[T/RC]}\, I_a(n) + [1/R]\, [V_o(n) - V_o(n-1)] \tag{7}$$

By the same manner, the block diagram shown in Fig. 5 represents the circuit illustrated in Fig. 1(b). The numerical recurrent relations of this block diagram can be deduced as:

$$V_C(n) = V_S(n) - V_o(n) \tag{8}$$

Using triangular hold without compensator, one obtains:

$$I_2(n) = [1/T]\,[V_C(n) - V_C(n-1)] \quad (9)$$
$$I_L(n) = I_2(n) - I_b(n) \quad (10)$$
$$V_o(n) = [1/T]\,[I_L(n) - I_L(n-1)] \quad (11)$$

Using zero order hold and e^{sT} compensator, one obtains:

$$I_b(n) = e^{-[RT/L]}\, I_b(n-1) - [1/R]\,\{e^{-[RT/L]}\}\, V_o(n) \quad (12)$$

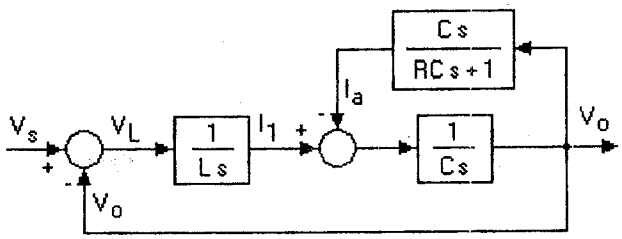

Fig. 5 The block diagram representation of the circuit in Fig. 1(b).

THE MOST ECONOMICAL UPS

General description

In the control scheme presented in Fig. 2, the inverter transistors may be derived to operate at 50 Hz. The resonance tank input voltage is a square wave but it delivers a constant sinusoidal current to the load due to the effect of high quality filtration of this tank. Therefore, the output voltage is also sinusoidal and depends on the value of the load impedance multiplied by the constant current value. The feedback signal maintains a constant output voltage at the load terminals by inversely changing the duty cycle of the inverter square wave input with respect to the load impedance magnitude. In this case, the UPS delivers a regulated sinusoidal output voltage. This mode of operation is the simplest one and the UPS is the most economical one. Because of the low switching frequency (50 Hz), the low cost power transistors can be used as inverter power switches.

Experimental results

The experimental setup described above has the component value mentioned in Appendix A. The load used can be considered as a resistive load because of its low inductance with respect to its resistance. Therefore, the UPS output terminals may be obtained across the capacitor or the inductor of the resonance tank.

The experimental input/output characteristic of the UPS (output voltage versus the duty cycle) is illustrated in Fig. 6. It is not a linear relation but it is a sinusoidal relation for duty cycle variation from 0 to 1.

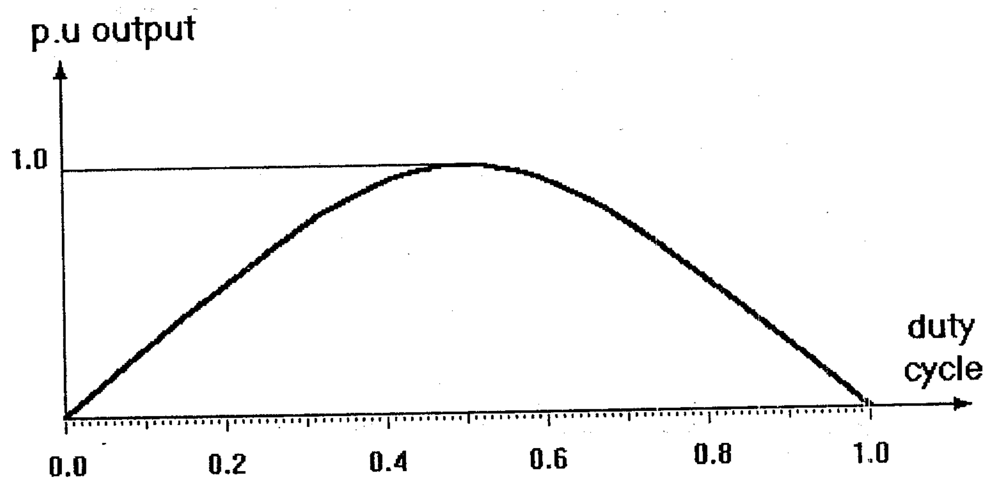

Fig. 6 The economical UPS input/output characteristic.

The economical UPS circuit variables are experimentally measured and illustrated in Fig. 7. The plotted curves shown can be described as:
plot (1): represents the voltage across the transistor T_1 with 5 V/div.
plot (2): illustrates the current through the transistor T_1 with 2 A/div.
plot (3): illustrates the current through the transistor T_2 with 2 A/div.
plot (4): represents the voltage across the capacitor (load) with 50 V/div.
The time base is 5 ms/div.

Another type of the economical UPS circuit variables are experimentally measured and illustrated in Fig. 8. The plotted curves shown can be described as:
plot (1): represents the voltage across the load terminals with 20 V/div.
plot (2): illustrates the current through the load resistance with 2 A/div.
plot (3): illustrates the current through the capacitor with 2 A/div.
plot (4): illustrates the current through the inductor with 2 A/div.
The time base is 5 ms/div.

<u>NB:</u> The experimental work has been carredout with a power supply has a current protection. This power supply output capacitor filter did not accept the long time period of 50 Hz operation of the UPS. Therefore, the current limitation is not due to the capability of the UPS but due to the output capacitor filter of the power supply.

Because of the natural resistance of the normal components used in the resonance tank and the power switch transistors, the no load resonance current is limited. This limited current flow through the capacitor or the coil impedance gives a limited UPS terminal voltage. In our UPS construction we found that the step up voltage ratio is of the resonance tank limited to about 10 times.

The main drawback of this economical UPS is its input/output nonlinear characteristic. Our concept is to design a PID controller of this UPS type. A duty cycle controlled symmetrical square wave generator is implemented to test the PID controller effect on the system output voltage performance. This control strategy is simulated, implemented and experimentally tested. Although the system non linearity, the designed PID controller achieves a wide range around the half load operating point.

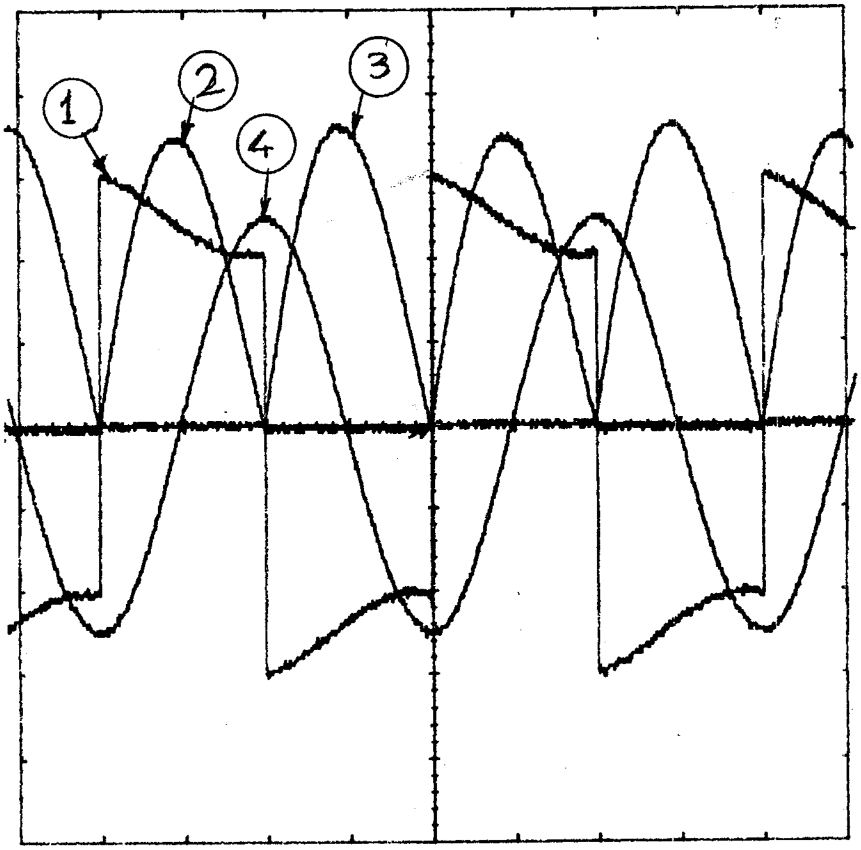

Fig. 7

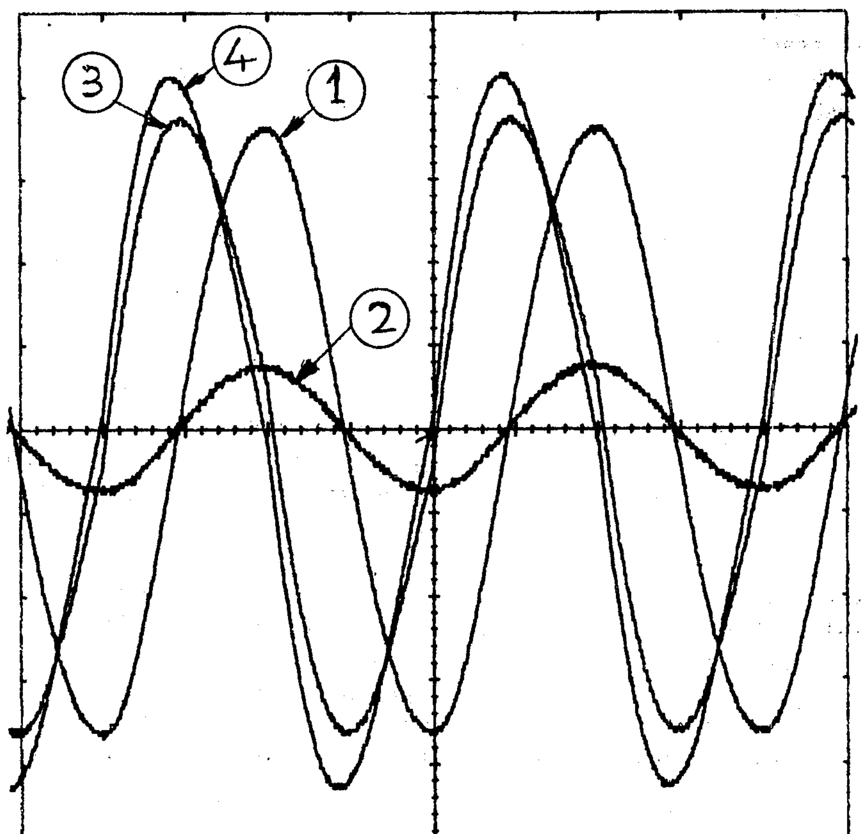

Fig. 8

HIGH PERFORMANCE UPS

General description

To reduce the size of the resonance tank components at one side and eliminate the nonlinear input/output characteristic of the UPS at the other side, a PWM technique has been applied to the UPS inverter. The resonance tank is modified to resonate at the PWM high frequency. Appendix B summarizes the UPS components values.

To apply the PWM technique on this type of UPS, a special circuit must replace the duty cycle variator. This circuit produces a sinusoidal distributed PWM pattern to drive the inverter power electronic switches. Figure 9 illustrates the construction of the sinusoidal distributed PWM pattern generator. In this generator, the frequency of the triangular wave is the PWM chopping high frequency and that of the sine wave is the operating frequency (50 Hz). The amplitude of the UPS output voltage depends on the ratio between the sine wave amplitude and the triangular wave amplitude. The input/output characteristic in this case is a linear relation. It is also found that if a triangular wave is used instead of the sine wave, the envelope of the UPS output voltage will be also a sinusoidal one. The generation of the triangular wave is more easy than the generation of the sine wave.

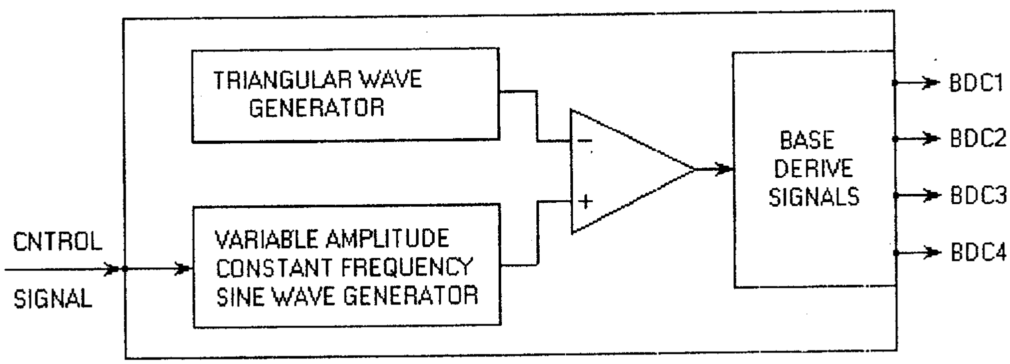

Fig. 9 The sinusoidal distributed PWM pattern generator.

Experimental results

The UPS output voltage in the PWM case is illustrated in Fig. 10. It is the chopping high frequency modulated by a sinusoidal envelope at the operating frequency. The plot shown in Fig. 10 represents the UPS output terminal voltage as a function of time. Voltage scale is 50 V/div. Time scale is 2.5 ms/div.

A selected variables of the PWM UPS are shown in Fig. 11. The plotted curves can be explained as:

plot (1): represents the voltage across the transistor T_1 with 10 V/div.
plot (2): illustrates the current through the inductor with 5 A/div.
plot (3): represents the voltage across the capacitor (load) with 100 V/div.
The time base is 10 µs/div.

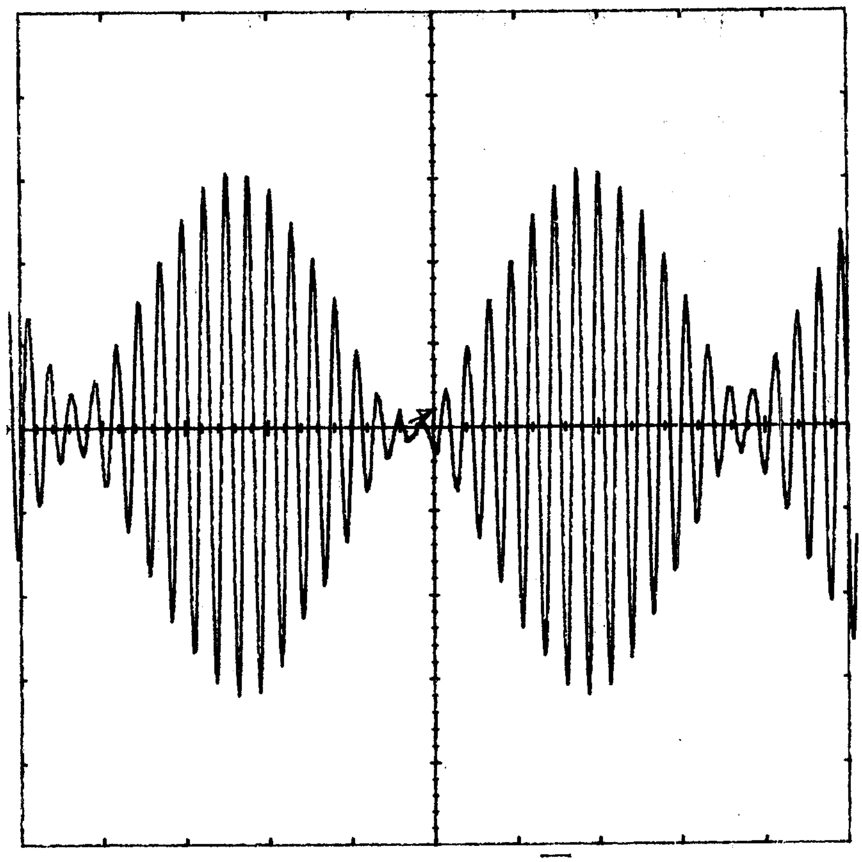

Fig. 10

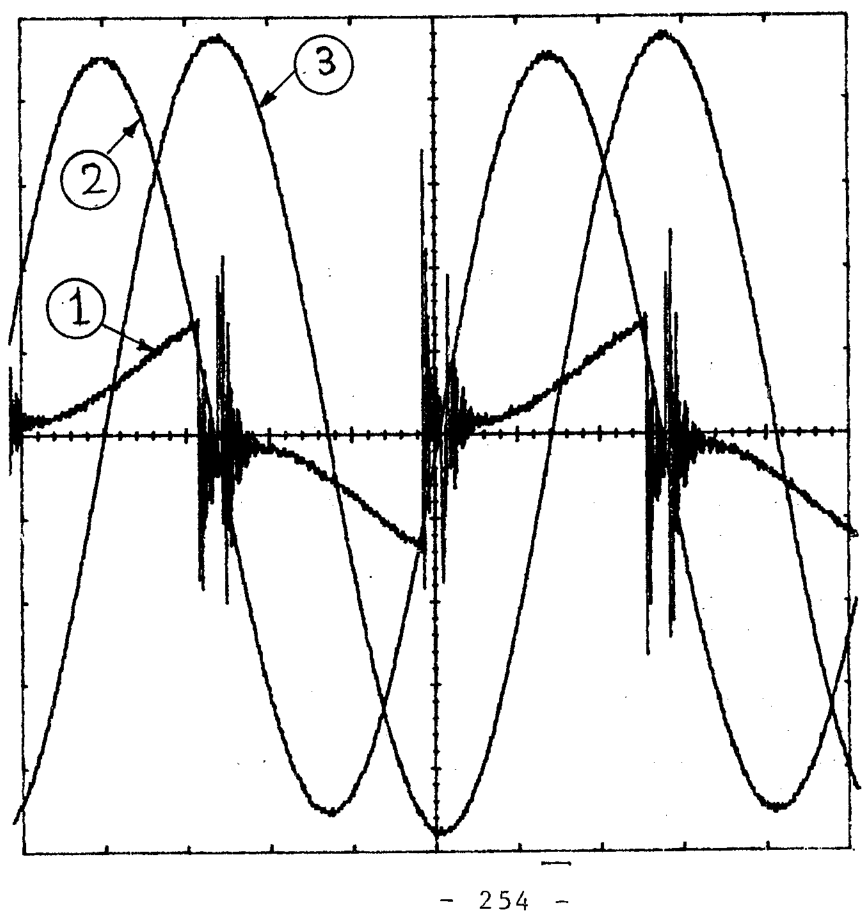

Fig. 11

This type of output voltage may be used as an AC sinusoidal voltage voltage through full bridge rectifier and another inverter operated at the low frequency (50 Hz). This type of circuits cannot recover the load reactive energy. Therefore, it is used only in the case of pure resistive loads. It can be mentioned here that; a special type inverter may be used to drive the non resistive loads [3]. The UPS output voltage and current are shown in Fig. 12. The plotted curves shown can be described as:

plot (1): represents the voltage across the load terminals with 100 V/div.
plot (2): illustrates the current through the load resistance with 500 mA/div.
The time base is 2 ms/div.

The time base stretched window shows the same load voltage and current of the marked area on plots (1) and (2) as illustrated below:

plot (3): represents the voltage across the load terminals with 100 V/div.
plot (4): illustrates the current through the load resistance with 500 mA/div.
The time base is 20 μs/div.

Using high frequency resonance tank in the UPS power circuit has the advantages of small size, light weight and low cost. The DC output voltage UPS can be constructed using the high frequency resonance tank. One type of DC output voltage UPS is experimentally tested during this work. The high frequency AC voltage across the UPS resonance tank terminals is rectified through a full bridge rectifier and filtered by a capacitor filter. This type of UPS gives the results shown in Fig. 13. The plotted curves can be explained as:

plot (1): represents the voltage across the load terminals with 50 V/div.
plot (2): illustrates the current through the load resistance with 500 mA/div.
plot (3): illustrates the current through the capacitor filter with 2 A/div.
plot (4): illustrates the current through the inductor with 2 A/div.
The time base is 10 μs/div.

To identify the global UPS system, a step response has been extracted at a partial load without output filter. The UPS response for the load voltage and current are shown in Fig.14. The plotted curves shown can be described as:

plot (1): the step input voltage is the standared TTL voltage with 5V/div.
plot (2): represents the voltage across the load terminals with 100 V/div.
plot (3): illustrates the current through the load resistance with 500 mA/div.
The time base is 200 μs/div.

Another identification response has been extracted for the UPS output voltage andcurrent with an output capacitor filter. This response is illustratd in Fig. 15. The plotted curves can be explained as:

plot (1): the step input voltage is the standared TTL voltage with 5V/div.
plot (2): represents the voltage across the load terminals with 50 V/div.
plot (3): illustrates the current through the load resistance with 200 mA/div.
The time base is 500 μs/div.

The system response shown in Fig. 14 and Fig. 15 are used to extract the necessary system parameters to calculate the PID controller settings. Ziegler and Nichol's method is applied to the UPS controller. The system performance is improved due to the application of designed PID controller.

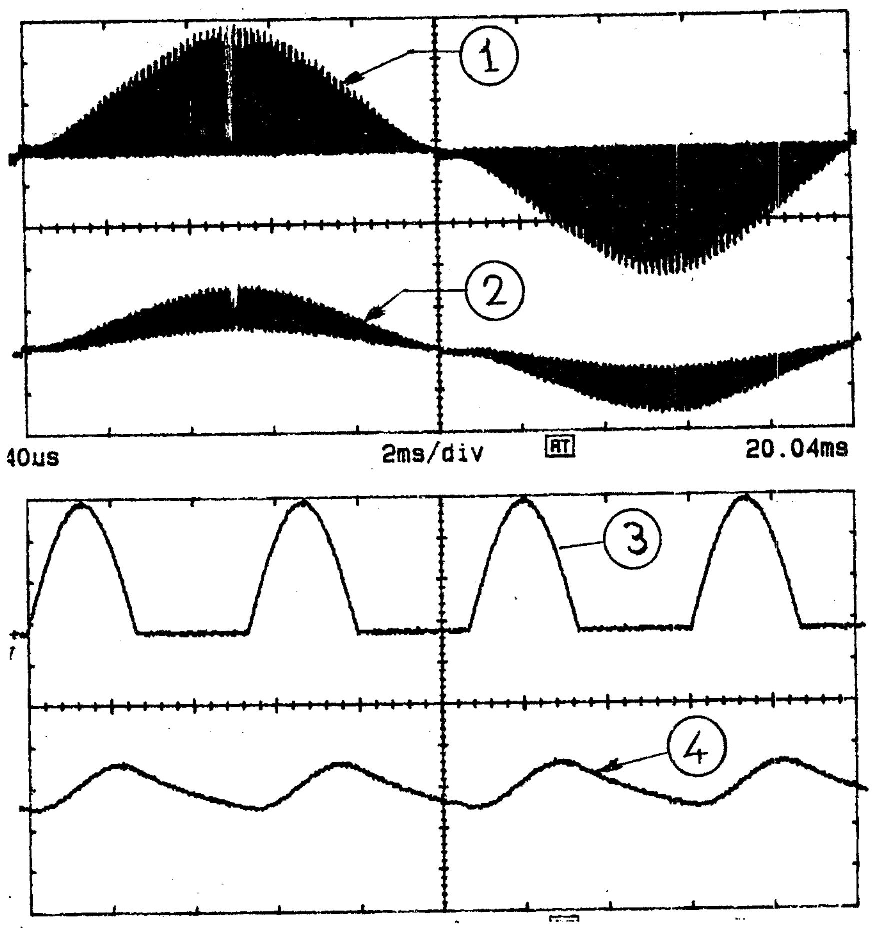

Fig. 12

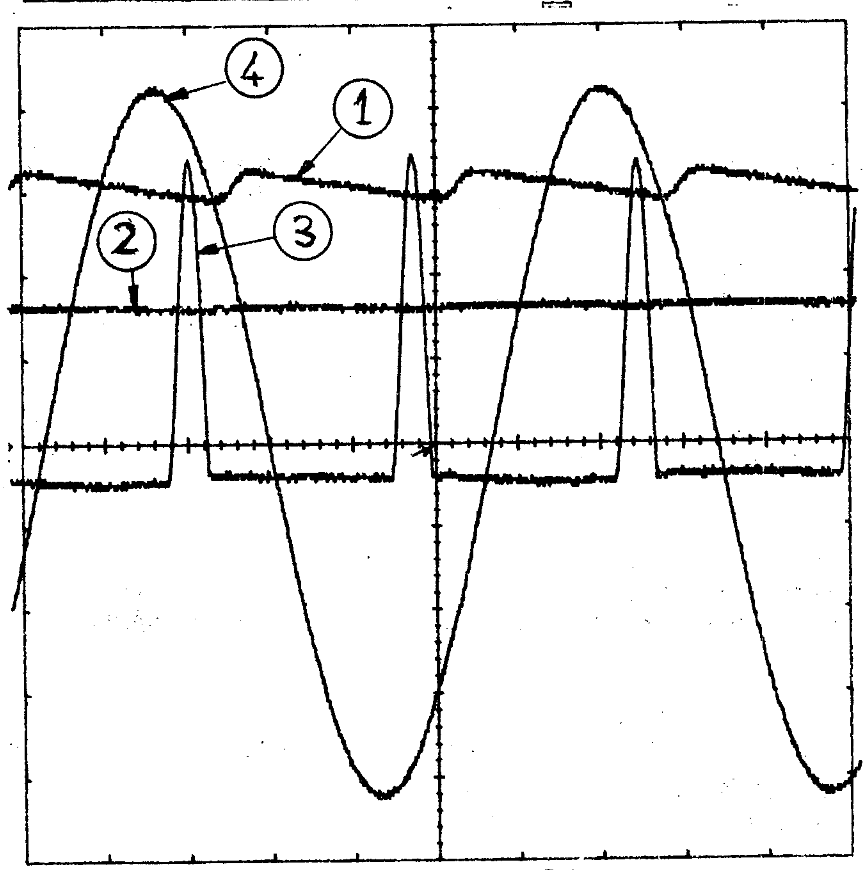

Fig. 13

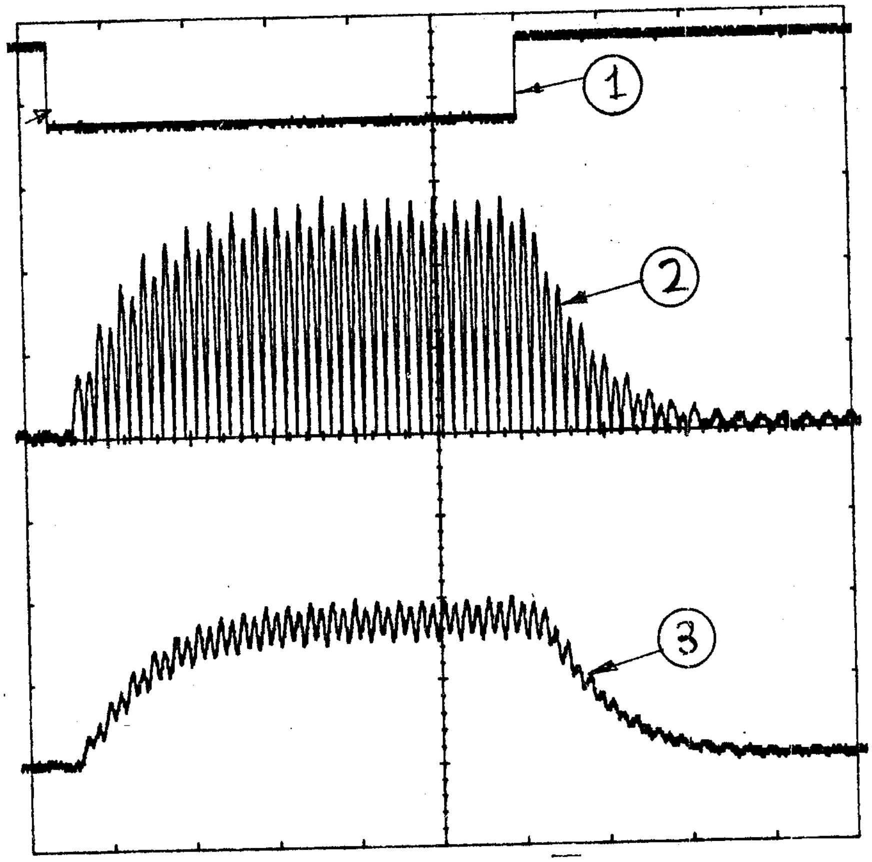

Fig. 14

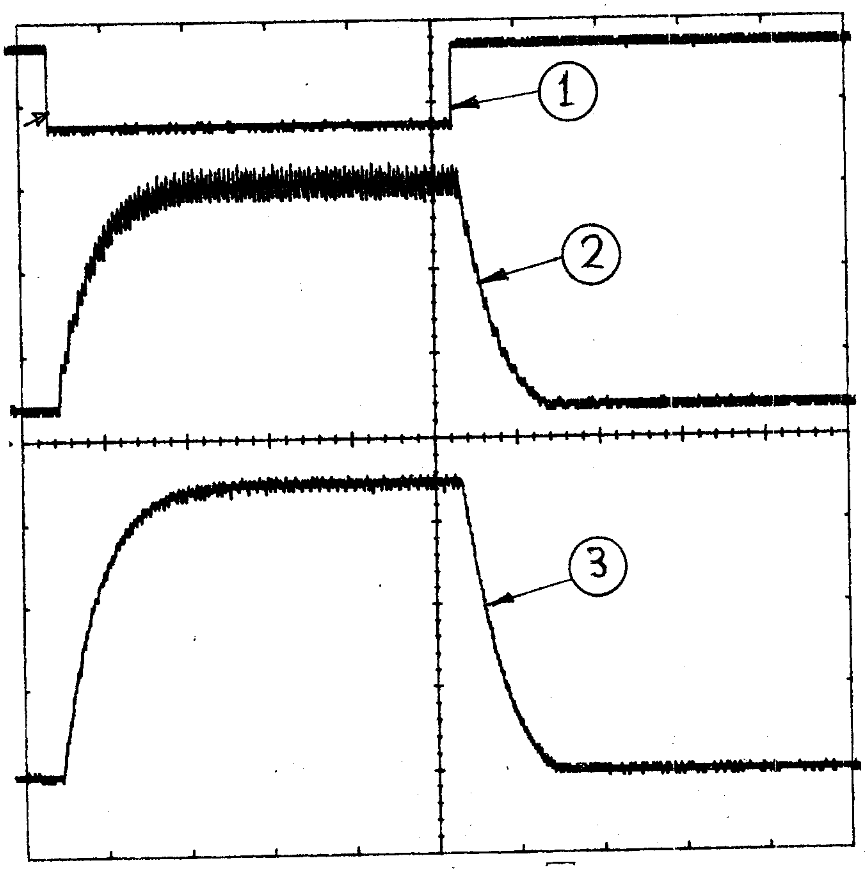

Fig. 15

CONCLUSION

This paper has demonstrated the application of a new design approach to the low power UPS in order to obtain a low cost transformerless UPS. This design technique can be applied to both the sinusoidal or DC output voltage . Theoretical studies, practical implementation and experimental work have been presented to show the use of a parallel loaded resonance circuit operated at its no load resonance frequency. The circuit duality of the resonance tank has been suggested and discussed. Application of the circuit duality gives design flexibility and eliminates the parallel resonance between the load, which is normally inductive, and the resonance tank output capacitor. Two techniques were applied to drive the resonance tank inverter. The first is the operation at the power network frequency (50 Hz). The second is The PWM technique at a high frequency. A low cost sinusoidal output voltage UPS was implemented and experimentally tested using the first technique. The output voltage of this UPS can be regulated. However, the step up voltage ratio is limited to about 10 times due to the natural resistance of the normal components used. The second technique has been used to reduce the size, weight and cost of the resonance tank. In this case, the UPS was used as an AC sinusoidal voltage for the resistive loads. The high frequency resonance tank was used to implement a DC output voltage because of its advantages. The system response and parameters were experimentally extracted to design the suitable controller for each implemented UPS. A special computer aided design program for the simulation of each UPS has been used in this work. Each program was used to determine the construction and suitable dimensions the UPS components. An acceptable accordance among the theoretical, simulation and experimental results during this work.

ACKNOWLEDGMENT

The author wishes to acknowledge his gratitude to: Mr. J-C. SABONNADIER, director of "Laboraroire d'Electrotechnique de Grenoble" (LEG), Mr. R. PERRET, vice-director of (LEG) and Mr. C. MASSELOT, director of "Ecole National Superieure des Ingenieurs Elecricians d'Grenoble" (ENSIEG); at the "Institut National Polytechnique de Grenoble" (INPG) in grenoble, France, for their assistants to realize this work. They offered the components, measuring equipment, computer facilities, bibliography and the place during the practical implementation and experimental work. He is also grateful to the staff member engineers and technicians of the research in the (LEG) for their valuable discussions during the period of this work.

APPENDICES

Appendix A

The components of the most economical UPS are:

1. The resonance tank inductor used is an air core coil that has
   - (a) inductance L = 54.7 mH.
   - (b) resistance R_L = 4.8 Ω DC measured.
2. The resonance tank capacitor is non polarized one that has
   - (a) capacitance C = 184.5 μF at 10 kHz.
   - (b) resistance R_C = 0.095 Ω at 10 kHz.

3. The load is a wire wound resistance that has
   (a) resistance R_{Ld} = 91.9 Ω DC measured, R_{Ld} = 93.74 Ω at 10 kHz.
   (b) self inductance L_{Ld} = 2.6 mH.

Appendix B

The high performance UPS has a resonance tank that was made for a high frequency operation. The coil of this resonance tank is an air core one that was made from Litz wire to eliminates the skin effect. This type of wire has the following construction: {200 isolated wires of 0.07 mm diameter which gives 0.77 mm^2 and 1.5 mm external diameter}.

1. The resonance tank inductor used has
   (a) inductance L = 154.8 mH.
   (b) resistance R_L = 0.234 Ω DC or 10 kHz measured.
2. The resonance tank capacitor is non polarized one that has
   (a) capacitance C = 473.5 nF at 10 kHz.
   (b) resistance R_C = negligible at 10 kHz.
3. The load is a wire wound resistance that has
   (a) resistance R_{Ld} = 188.0 Ω DC measured, or R_{Ld} = 191.5 Ω at 10 kHz.
   (b) self inductance L_{Ld} = 5.55 mH at 10 kHz.
4. Capacitor filter in the case of DC output voltage UPS is non polarized one that has:
   (a) capacitance C = 1.035 μF at 10 kHz.
   (b) resistance R_C = negligible at 10 kHz.
5. Inverter and resonance tank operating frequency is 18.50 kHz.
6. Load operating frequency in the case of sinusoidal output voltage UPS is 50 Hz.

REFERENCES

[1] EMSERMANN M.," Analysis and design of a sinusoidal power converter ", EPE'89 - Aachen - Germany, Vol. I, pp. 331 - 336, 9 - 12 October 1989.

[2] YONEMORI H., NISHIDA Y., NAKAOKA M., and HARASHIMA F.," Instantaneous voltage control based sinusoidal CVCF inverter with high frequency resonance AC link and in UPS system applications ", EPE'89 - Aachen - Germany, Vol. I, pp. 341 - 346, 9 - 12 October 1989.

[3] BRUNELLO M., FERRIEUX J-P. and PERARD J.," Use of resonance devices in uninterruptable power supplies ", EPE'89 - Aachen - Germany, Vol. II, pp. 683 - 688, 9 - 12 October 1989.

[4] EL-GHOTMY M. A., IBRAHIM S.A. and MAHMOUD M.I.," A new design approach of the parallel resonance inverters for a high power constant current source ", Engineering Research Bulletin, shebin el - kom, Vol. XIII, part 1, pp. 53 - 63, 1991.

[5] MAHMUOD M. I., BARBAROUX J., PERRET R.," Constant current mode for parallel loaded resonance circuit inverter: AC and DC applications ", EPE'91 - Florence - Italy, Vol. III, pp. (3 - 310) to (3 - 315), 3 - 6 September 1991.

[6] SMITH J. M.," Mathematical modeling and digital simulation for engineers and scientists ", JOHN WILEY and SONS Publication, 1977.

الملخص:

فى الوقت الحالى يأخذ موضوع البحث فى مجال مصادر التغذية بالقدرة غير المنقطعة (Uninterruptable Power Supply, UPS) إقبالا وإهتماماً شديداً من كثير من الباحثين. القدرات الصغيرة لهذا النوع من مصادر التغذية غير المنقطعة يلقى إهتماماً خاصاً داخل هذا المجال من البحوث. مصادر القدرة من هذا النوع ذات القدرات الصغيرة تجد تطبيقاً واسع الإنتشار فى مجال الحاسبات الشخصية وتطبيقاتها العملية وبوجه خاص فى العمليات الصناعية.

يقدم المؤلف فى هذا العمل طريقة تصميم جديدة لتطبيقها فى مجال مصادر التغذية بالقدرة غير المنقطعة فى حالة القدرات المنخفضة حينما يكون جهد الخرج مستمر أومتردد جيبى. أجريت خلال هذا العمل دراسات نظرية لحقها تطبيقات عملية على دائرة رنين تعمل على تردد الرنين لها عند حالة اللاحمل بغرض إستخدام خاصيتها فى دفع تيار جيبى ثابت خلال الحمل عند تحميلها. يمكن تشغيل دائر الرنين هذه عن طريق عاكس الكترونيات القدرة (Power Electronic inverter) إما بواسطة موجة مربعة تعمل بتردد قيمته تردد شبكة التغذية بالقدرة أو بواسطة طريقة تغيير عرض النبضات (Pulse Width Modulation, PWM) على تردد عال. إستخدمت تقنية تردد شبكة التغذية بالقدرة لتقليل مكونات الكترونيات القدرة ودوائر التحكم فيها أما تقنية تغيير عرض النبضات فقد إستخدمت لتقليل حجم دائر ة الرنين المتخدمة فى النظام. نتيجة للبحث النظرى والتنفيذ العملى والإختبارات والقياسات المعملية تبين بواسطة هذا البحث حدود تصميم هذا النوع من الأنظمة وكذلك أبعاد عناصره المستخدمة.

إقترح خلال هذا العمل تطبيق خاصية الإزدواجية (Duality Characteristic) على دائرة الرنين المستخدمة. بدراسة هذه الخاصية أمكن الوصول إلى مرونة فى التصميم لهذا النوع من النظم وذلك بتلافى ظاهرة رنين التوازى بين الحمل ومكثف الخرج لدائرة الرنين. تم تصميم وتنفيذ برنامج خاص يعمل على الحاسب الآلى لتمثيل النظام قيد البحث فى الحالات المختلفة التى تمت دراستها خلال هذا العمل. أمكن عن طريق هذا البرنامج تحديد الأبعاد وإختيار العناصر المناسبة لتكوين عاكس الكترونيات القدرة ودائرة الرنين للنظام فى حالات إنتاج الجهد المتردد الجيبى والجهد المستمر.

لتحديد هوية النظام الفعلى أجريت تجارب معملية لقياس وتسجيل الإستجابات العابرة للنظام ام فى الحالات المختلفة التى تمت دراستها وعند حالات التحميل المختلفة لكل منها. هذه الإستجابات العابرة حددت إختيار وتركيب الحاكمات (Controllers) الواجب إستخدامها مع النظام فى حالاته المختلفة بغرض الحصول على نظم ذات خواص عالية الجودة. هناك تطابق بين النتائج النظرية وبرنامج تمثيل النظام من ناحية ونتائج القياسات والإختبارات العملية والمعملية على النظام فى الحالات المختلفة التى تمت دراستها خلال هذا العمل.