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A Modified Modular Multilevel Converter with Reduced Number of Power Electronic Components

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ABSTRACT

This paper presents a modified multilevel inverter with a few number of semiconductor switches and increasing number of output levels. One stage of the proposed inverter leads to get seven levels in the output voltage, while, forty-nine levels can be obtained when using two stages. Only six semiconductor switches are required for each stage. Standard DC sources are used, so, DC-DC converter is not required to get the desired output standard voltage. Total harmonic distortion in the output waveform of the two stage inverter is very low, so, using filter to improve output waveform is unnecessary. This topology is valid for all types of loads. Simulation results are presented for one stage and two stage inverters proposed. Experimental results are included for the one stage inverter to verify the theoretical results.

يقدم هذا البحث تصميم معدل لعاكس جهد متعدد المستويات باستخدام عدد اقل من المفاتيح الاليكترونية مع اعطاء عدد اكثر من المستويات في جهد الخرج. يمكن الحصول علي سبعة مستويات في جهد الخرج عند استخدام مرحلة واحدة من هذا العاكس بينما استخدام مرحلتين منه يؤدي الي الحصول علي تسعة واربعون مستوي. كل مرحلة من العاكس تتطلب ستة مفاتيح فقط. الجهود المستمرة المستخدمة ذات قيم قياسية لذلك لا حاجة لاستخدام مغير جهد مستمر للحصول علي جهد خرج قياسي. تشويه التوافقيات الكلي في موجة خرج العاكس ذو المرحلتين قيمته منخفضة جدا لذلك استخدام مرشح توافقيات لتحسين موجة الخرج غير ضروري. ويعد هذا العاكس المقترح صالح لكل انواع الاحمال. وتم تقديم النتائج النظرية للعاكس ذو المرحلة الواحدة والعاكس ذو المرحلتين. وقدمت النتائج العملية للعاكس ذو المرحلة الواحدة لتحقيق النتائج النظرية.

Key words: *Multilevel inverter, Reduced number of power electronic component, Total harmonic distortion.*

I. INTRODUCTION

In recent years, power electronic inverters are becoming very important for many applications such as, motor controlling and power systems [1, 2]. In last years, multilevel inverters have been received increasing attention due to many advantages such as, high quality output waveform, low value of the voltage stress on switches, lower switching losses and higher efficiency[3]. The general concept of multilevel inverters involves utilizing a higher number of active semiconductor switches to perform the power conversion in small voltage steps. Multilevel inverters are used extensively in medium and high power applications such as static reactive power compensation and adjustable-speed drives [4, 5]. The applications of multilevel inverters have also extended to low power applications such as photovoltaic system and hybrid electrical vehicles [6, 7].

Multilevel inverters can be divided into three basic topologies which are the neutral point clamped (NPC), the flying capacitor (FC) and the cascaded H-bridge (CHB). The NPC is the first generation of multilevel inverters presented by Nabae [8] which have three levels. The main disadvantages of NPC are unequal voltage sharing between series connected capacitors that result in unbalancing of dc-link capacitors and requiring additional clamping diodes. The FC multilevel inverter uses flying capacitors as clamping devices [9]. This topology has advantages in comparison with the NPC multilevel inverters such as equal voltage sharing between semiconductor switches. But, for high voltage steps, this topology requires a high number of storage capacitors. The CHB multilevel inverters consist of H-Bridge cells, with an isolated dc source connected to each cell,

connected in series. This topology is proper for high level applications from point of view of modularity and simplicity of control. From the view point of values of dc voltage source, The CHB multilevel inverters are divided into two main groups, the symmetric and asymmetric topology. In the symmetric topology, all dc input voltage sources have equal values. This feature makes the topology good modularity but gives a few number of levels in the output waveform compared with the asymmetric topology in which, dc voltage source are different in such manner to give more output voltage levels [10, 11].

The main disadvantage of multilevel inverters is the large number of semiconductor switches required. Thus, many efforts have been focused to construct new topologies of multilevel inverters with less number of semiconductor switches [12, 13, 14]. A new constructed multistring multilevel inverter was proposed in [13]. This new design of multilevel inverter presents a transformerless five-level multistring inverter for fuel-cell micro grid system. Simplified multilevel inverter proposed in [13] uses only six semiconductor switches instead of eight used in conventional cascaded H-Bridge inverter. However, a step-up converter and L-C filter are required in this topology.

In this paper a two modified modular multilevel inverters are presented, the one stage inverter and two stage inverter. The one stage inverter uses six semiconductor switches and two dc sources with unequal value producing output waveform with seven levels instead of five in case of symmetric dc sources [13]. The two stage inverter requires only twelve switches and four dc sources with a certain ratio giving output voltage with 49 levels. Thus, harmonics in the output voltage is very low without using filter. Cascaded H-Bridge multilevel inverter with the same number of semiconductor switches ,twelve switches, produce 7-levels waveform in case of symmetric dc sources and 27-levels in case of asymmetric dc sources with ratio (1: 3: 9) [15]. Thus, the presented topology has low number of switches with more number of output levels compared with other topologies. Variation of output voltage and frequency are available in this topology. The descriptions and the operating principals of the two multilevel inverters proposed are included in this paper. A simple technique of control is used for this topology that makes it valid for different types of loads. Simulation and experimental results are included to verify the effectiveness of the modified topology proposed.

II. SYSTEM DESCRIPTION AND PRINCIPAL OF OPERATION

A. One Stage Inverter

To increase the number of output levels, additional power electronic components are required as it is well known. This leads to increasing in size, cost, losses and control complexity. A modular modified inverter is presented in this paper to increase the number of level without increasing number of switches. The number of output levels given by this multilevel inverter is:

$$N_{level} = 2\left(\frac{V_{dc1} + V_{dc2} + \ldots\ldots + V_{dcn}}{V_{dc1}}\right) + 1 \quad (1)$$

The peak value of output voltage is:

$$V_{peak} = V_{dc1} + V_{dc2} + \ldots\ldots + V_{dcn} \quad (2)$$

Where n is the number of dc sources.

The power circuit of the one stage inverter proposed is shown in fig. 1 . It consists of only six semiconductor switches and two dc sources.

For symmetric dc sources where, $V_{dc1}=V_{dc2}=V_s$:

$$N_{level} = 2\left(\frac{V_s + V_s}{V_s}\right) + 1 = 5 \text{ levels} \quad (3)$$

The peak value of output voltage:

$$V_{peak} = V_s + V_s = 2\ V_s . \quad (4)$$

Thus, maximum number of voltage levels can be produced in this case is five level ($+2V_s$, $+V_s$, 0, $-V_s$, $-2V_s$).

For asymmetric dc sources with ratio (1:2) where, $V_{dc1}=V_s$ and $V_{dc2}=2V_s$:

$$N_{level} = 2\left(\frac{V_s + 2V_s}{V_s}\right) + 1 = 7 \text{ levels} \quad (5)$$

The peak value of output voltage:

$$V_{peak} = V_s + 2V_S = 3\ V_s . \quad (6)$$

Two additional levels are added to output voltage in this case. So, seven levels can be produced from this inverter by different combination of switching operation as follow:

(a) Maximum positive level, $+3V_s$: the on switches in this state are S2, S4 and S6.
(b) For output level, $+2V_s$: this level can be obtained when the switches S1, S2 and S6 are on.
(c) For output level, $+V_s$: the on switches are S2, S3 and S4.
(d) For zero output, $0V_s$: this condition can be obtained by two different ways. The first by making

the left leg on, S1, S2 and S3. the second by making the right leg on, S4, S5 and S6.
(e) Negative level, $-V_s$: this level can be induced when the switches S1, S5 and S6 are on.
(f) For output voltage $-2V_s$ the on switches are S3, S4 and S5.
(g) Maximum negative level, $-3V_s$: the on switches are S1, S3 and S5.
Typical output wave form of one stage inverter with asymmetric dc sources is shown in Fig. 2.

B. Two Stage Inverter analysis

The power circuit of the modified multilevel inverter is shown in Fig. 3. This system consists of two stages of multilevel inverter shown in Fig.1 connected in series. The system proposed involves only twelve semiconductor switches and four dc sources with unequal values. The voltage sources are chosen as standard values so, dc to dc converter is not required. Transformer is not required in this

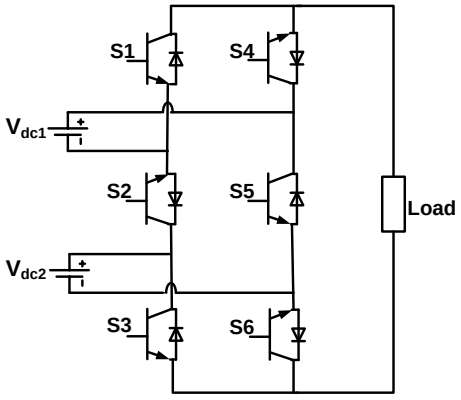


Fig. 1 one stage multilevel inverter

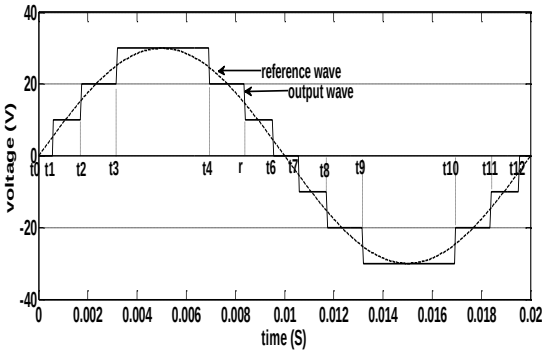


Fig. 2 typical output wave form of one stage inverter

system as the output voltage is standard value as shown in results. Total harmonic distortion (THD) has a low value, within the standard value, thus, L-C filter is not required. The ratio between the values of the dc sources is chosen to give maximum number of levels of the output waveform. It is found that the optimum ratio between voltage sources is (1: 2: 7: 14). This ratio leads to get forty-nine levels from the two stage inverter proposed.
To obtain the maximum number of output levels with symmetrical difference, the ratio between the values of the dc voltage sources should be 1: 2: 7: 14

The total number of levels in the output wave form according to equation (1) is:

$$N_{level} = 2(\frac{V_s + 2V_s + 7V_s + 14V_s}{V_s}) + 1 = 49 \text{ levels}$$

(7)
The peak value of output voltage according to equation (2) is:

$$V_{peak} = V_s + 2V_S + 7V_s + 14V_s = 24\ V_s .$$

(8)
Where V_s is the value of the first voltage source (V_{dc1}).

These output levels can be obtained as follow:

(1) For zero output, this output state can be obtained by two switching combination. Once switches combination is making the switches S1, S2, S3, S7, S8 and S9 on. The other combination is making S4, S5, S6, S10, S11 and S12 on.

(2) For output voltage V_s, $V_o = V_{dc1} = V_s$,
The on switches are S2, S3, S4, S7, S8 and S9.

(3) For output voltage $2V_s$, $V_o = V_{dc2} = 2V_s$, the switches S1, S2, S6, S7, S8 and S9 are on.

(4) For output voltage $3V_s$,
$V_o = V_{dc1} + V_{dc2} = V_s + 2V_s = 3V_s$
The on switches are S2, S4, S6, S7, S8 and S9.

(5) For output voltage $4V_s$,
$V_o = V_{dc3} - (V_{dc1} + V_{dc2}) = 7V_s - (V_s + 2V_s) = 4V_s$
The on switches are S1, S3, S5, S8, S9 and S10.

(25) For maximum positive output voltage $24V_s$,
$V_o = V_{dc1} + V_{dc2} + V_{dc3} + V_{dc4} = V_s + 2V_s + 7V_s + 14V_s = 24V_s$
The on switches are S2, S4, S6, S8, S10 and S12.

(26) For output voltage $-V_s$, $V_o = -V_{dc1} = -V_s$,
The on switches are S1, S5, S6, S10, S11 and S12.

(27) For output voltage $-2V_s$, $V_o = -V_{dc2} = -2V_s$,
The on switches are S3, S4, S5, S10, S11 and S12.

(28) For output voltage $-3V_s$,
$V_o = -(V_{dc1} + V_{dc2}) = -(V_s + 2V_s) = -3V_s$,
The on switches are S1, S3, S5, S10, S11 and S12.

(29) For output voltage $-4V_s$,
$V_o = -V_{dc3} + (V_{dc1}+V_{dc2}) = -7V_s + (V_s+2V_s) = -4V_s$
The on switches are S2, S4, S6, S7, S11 and S12

(49) For maximum negative output voltage $-24V_s$,
$V_o = -V_{dc1}-V_{dc2}-V_{dc3}-V_{dc4} = -V_s -2V_s -7V_s -14V_s = -24V_s$
The on switches are S1, S3, S5, S7, S9 and S11.

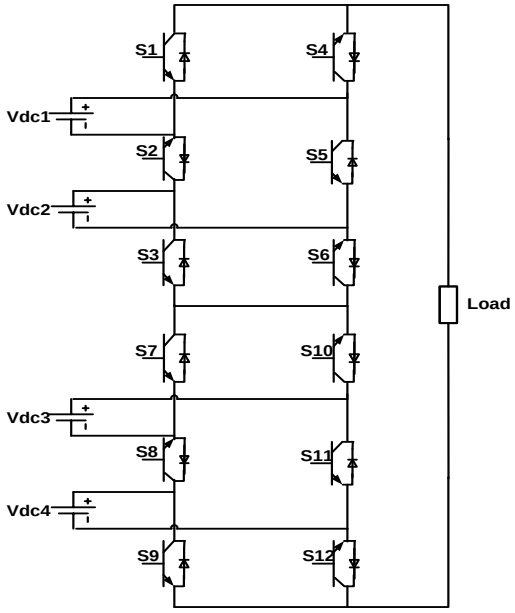


Fig. 3 two stage multilevel inverter

C. Switching Pulse System

A simple and new technique is used for pulse generation for this topology. This technique consists of four stages, reference sine wave signal, comparators, logic circuits and drive circuits as shown in Fig. 4. The reference signal has two inputs, reference voltage and frequency, to control the voltage and frequency of the output wave form. The comparators divide the reference signal into number of levels equal to the number of levels demanded in the output waveform. The comparators transfer from a level to the next when the reference sine wave reaches to mid-value between the two levels. Thus, output waveform always follows the reference sine wave producing wave with fewer harmonic with no need to output filter. The outputs of the comparators are considered as inputs to logic circuits which generate the pulses according to the switches required to be on for each level. Then, drive circuits are required to make pulses suitable for switches.

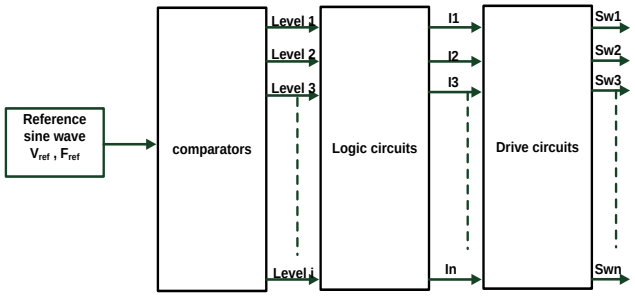


Fig. 4 block diagram of switching pulse system

III. SIMULATION RESULTS

The simulation studies are carried out for one and two stage inverter proposed in this paper. The MATLAB Simulink software has been used for simulation studies. The output voltage, load current and harmonics spectrum are examined for two systems.

A. Simulation Results of One Stage Inverter

The one stage inverter is modeled according to Fig. 1 and its control system to give output waveform with 50-HZ and 36 V (peak). The values of the dc sources is chosen as V_{dc1}=12V, V_{dc2}=24V. The simulation studies have been carried out for two types of loads, resistive and inductive loads.

For resistive load (R=14Ω), the waveform given in Fig. 5, 6 and 7 are output voltage, load current and harmonics spectrum respectively. Simulated output voltage has seven levels and follows the reference sine wave as shown. The load current have the same shape of voltage with the same THD ratio as the load is resistive and THD ratio in the output wave is 12.2%. Output voltage with load current is shown in Fig. 8.

For inductive load (R=14Ω and L=9mH), Fig. 9, 10 and 11 show output voltage, load current and harmonics spectrum of load current respectively. Output voltage is the same as the case of resistive load. Load current is smoother with low harmonics because of the load inductance. Harmonics spectrum of the output voltage is the same as shown in Fig. 7 and THD in the load current is 3.79%. load current lags output voltage due to the load inductance as shown in Fig. 12.

THD in the output voltage waveform of one stage inverter is still high, 12.2%, so this inverter may need L-C filter but with size less than in case of symmetric DC sources in [13]. Therefore, two stages are connected in series to give 49-level inverter proposed in this paper which reduce THD.

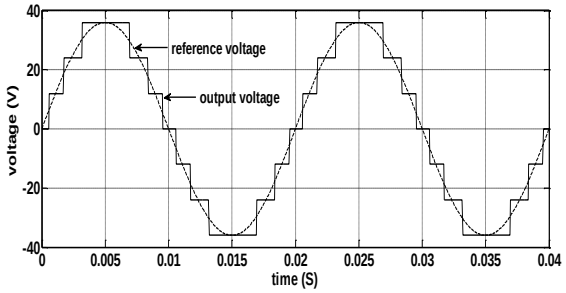


Fig. 5 simulated output voltage for resistive load

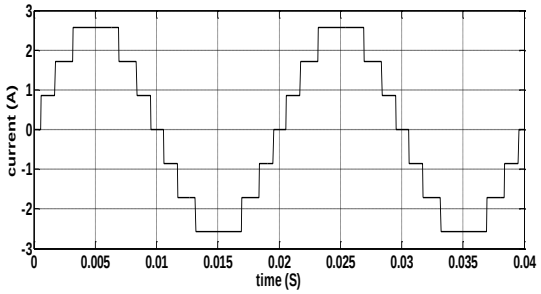


Fig. 6 simulated load current for resistive load

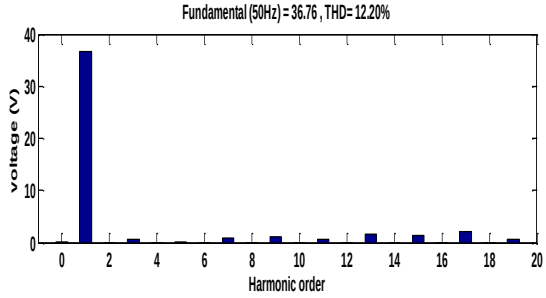


Fig. 7 harmonics spectrum of the output waveform for resistive load

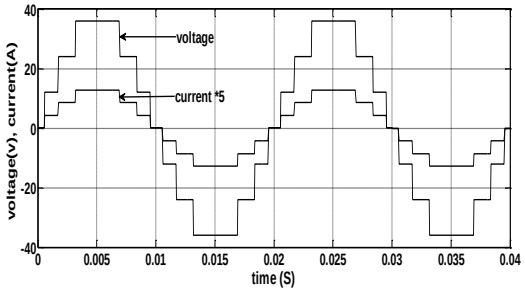


Fig. 8 Simulated output voltage with load current for resistive load

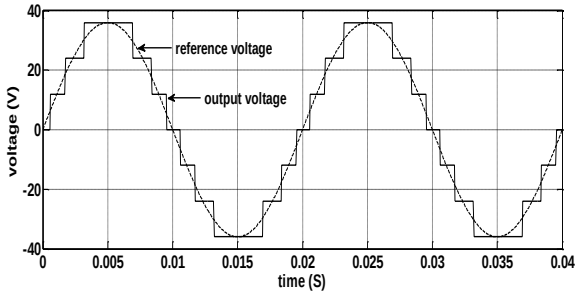


Fig. 9 simulated output voltage for inductive load

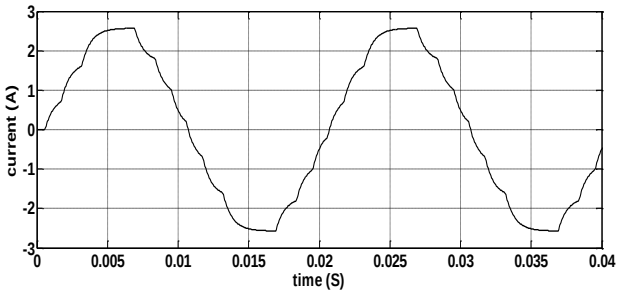


Fig. 10 simulated load current for inductive load

B. Simulation Results of Two Stage Inverter

The model of the two stage inverter shown in Fig. 3 is implemented with its switching pulse system using MATLAB- Simulink. The ratio between values of the dc

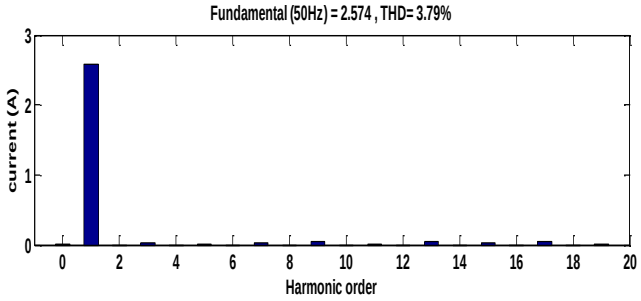


Fig. 11 harmonics spectrum of the load current for inductive load

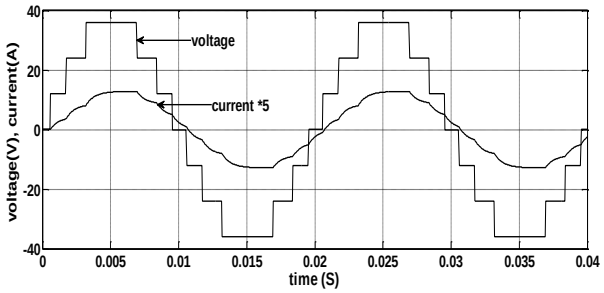


Fig. 12 Simulated output voltage with load current for inductive load

voltage sources should be 1:2:7:14 as illustrated before. When the value of the first voltage source V_{dc1}=12V this give output waveform with maximum value 288V according to equation (2)

$$V_{peak} = 12 + 2\times12 + 7\times12 + 14\times12 = 288 \text{ V}.$$

The RMS value is $= \frac{288}{\sqrt{2}} = 203.6 \text{ V}.$

In this case the input dc voltages have a standard values but output ac voltage value is not standard. So, small change in the voltage ratio can give standard output voltage 220V (RMS). The modified ratio of dc

voltage sources is 1:2:8:15. The maximum value of the output voltage in this case is:

$$V_{peak} = 12 + 2\times12 + 8\times12 + 15\times12 = 312 \text{ V}$$

The RMS value is $= \frac{312}{\sqrt{2}} = 220.6$ V (standard value)

According to equation (1), the number of levels is:

$$N_{level} = 2(\frac{V_s + 2V_s + 8V_s + 15V_s}{V_s}) + 1 = 53 \text{ levels}$$

.

This modified ratio gives ac output standard voltage with input dc standard voltages. But, four voltage levels can not be obtained with this modified ratio. These levels are $4V_s$, $19V_s$, $-4V_s$ and $-19V_s$. This leads to a small increasing in THD but still within IEEE standard area.

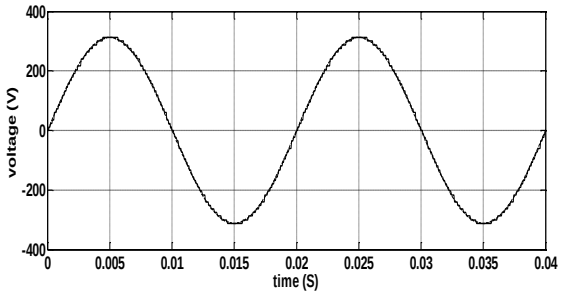
Simulation studies have been carried out with the parameter values as follow,

$V_{dc1} = 12V$, $V_{dc2} = 2\times12 = 24V$,

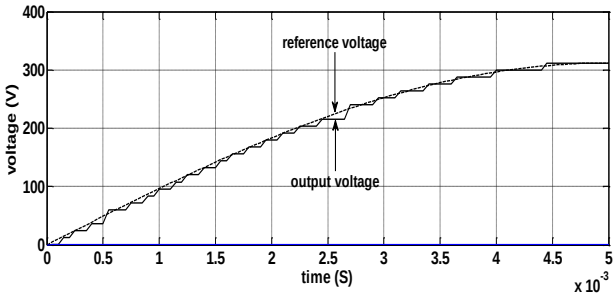
$V_{dc3} = 8\times12 = 96V$, $V_{dc4} = 15\times12 = 180V$.

For resistive load (R=14Ω), output voltage, load current and harmonics spectrum of the output wave are shown in Fig. 13,14 and 15 respectively. Fig. 13(a) shows output voltage having forty-nine levels with the reference sine wave. It is clear that output wave and reference sine wave are typical. Fig. 13(b) shows a quarter cycle of output voltage to illustrate the levels clearly. The load current wave is shown in Fig. 14 have a forty-nine levels as voltage wave because the load is resistive. Harmonics spectrum of the output voltage is shown in Fig. 15 with THD ratio 1.8%. simulated output voltage with load current for resistive load is shown in Fig. 16.

For inductive load (R=14Ω and L=9mH), Fig. 17, 18 and 19 show output voltage, load current and harmonics spectrum of the load current. Output voltage for inductive load and resistive load are the same. So, Harmonics order values of output voltage for inductive load is the same as shown in Fig. 15. The load current wave is improved due to the inductance of the load as shown in Fig. 18. THD ratio of load current is 0.18% as shown in Fig. 19.



(a)



(b)

Fig. 13 (a) simulated output voltage for resistive load, (b) quarter cycle of output voltage

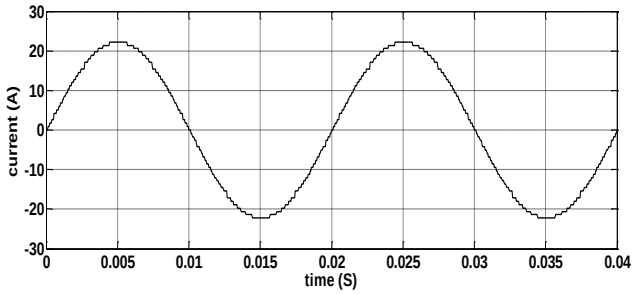


Fig. 14 output voltage with load current for inductive load

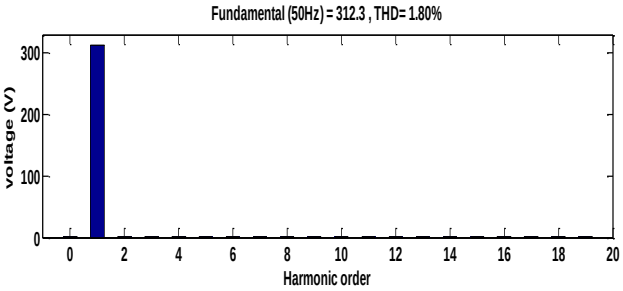


Fig. 15 harmonic spectrum of simulated output waveform for resistive load

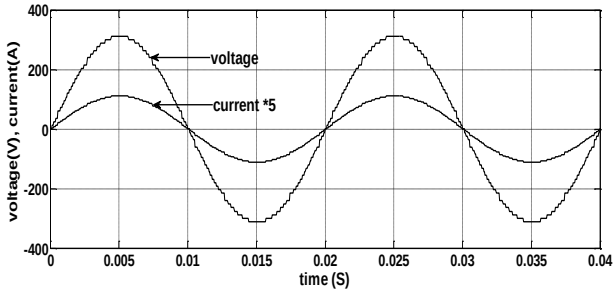
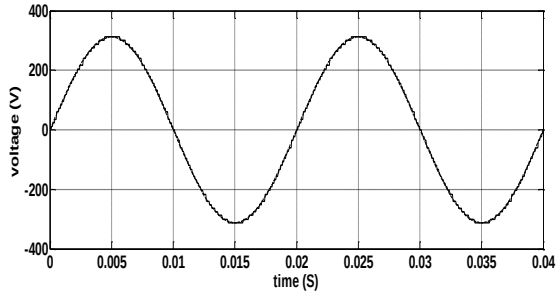
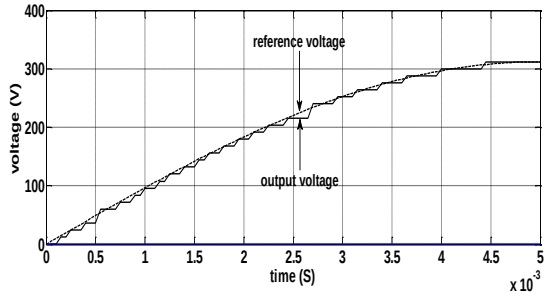


Fig. 16 Simulated output voltage with load current for resistive load



(a)



(b)

Fig. 17 (a) simulated output voltage for inductive load, (b) quarter cycle of output voltage

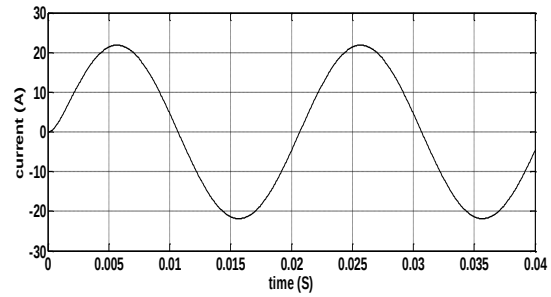


Fig. 18 simulated load current for inductive load

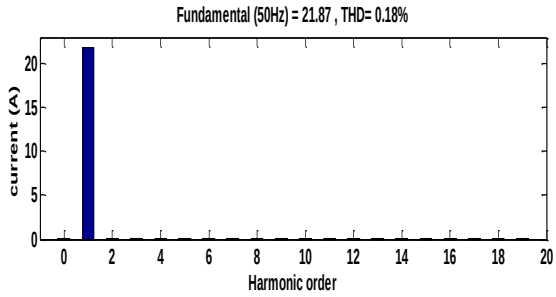


Fig. 19 harmonics spectrum of the load current for inductive load

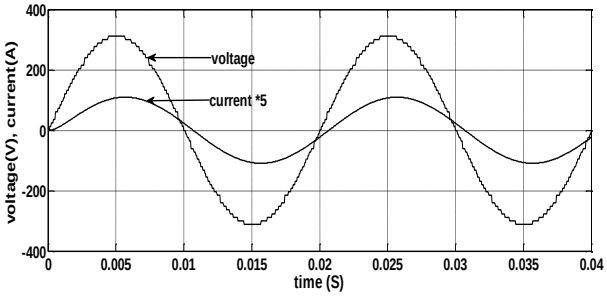


Fig. 20 simulated output voltage with load current for inductive load

IV. EXPERIMENTAL RESULTS

The prototype of one stage inverter is set up in laboratory and the performance is examined through experimental tests to verify the concept proposed. Digital signal processor (DSP1103) is used for control system. Mitsubishi IGBT Modules are used as switches in the power circuit. The performance of one stage inverter is examined as a stage in the two stage inverter proposed. Results are taken for two types of loads, resistive load (R=14Ω) and inductive load (R=14Ω and L=9mH). The values of dc sources used in experimental tests are the same used in simulation where V_{dc1}=12V, V_{dc2}=24V.

For resistive load, output voltage and load current are shown in fig. 21 and 22. Output voltage wave have seven levels with peak value approximately (35 V) and follows the reference sine wave as shown in Fig. 21. Load current have also seven levels as shown in Fig. 22. Fig. 23 shows output voltage with load current for resistive load. In case of inductive load, Fig. 24, 25 and 26 show output voltage, load current and output voltage with load current respectively.

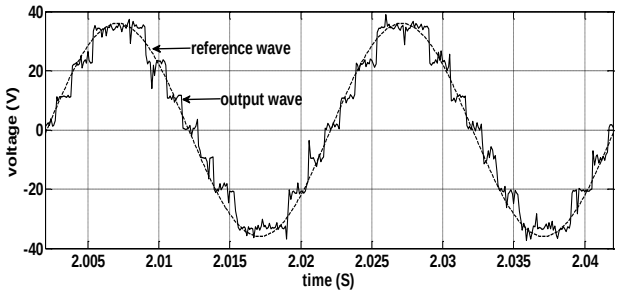


Fig. 21 Experimented output voltage for resistive load

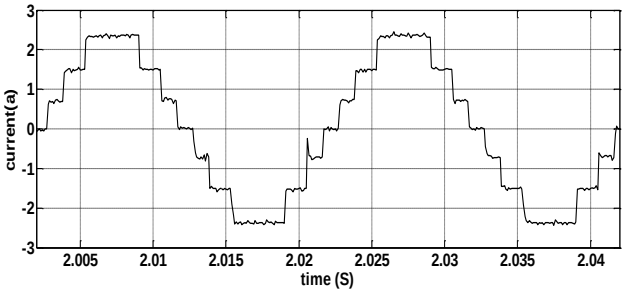


Fig. 22 experimented load current for resistive load

V. CONCLUSION

A new design of multilevel inverter has been proposed. The proposed system uses the reduction of power electronic switches used, power losses and cost. The number of output levels can be increased by adding an additional stage with a certain ratio of voltage sources. So, this topology is convention for expanding. THD in the one stage inverter is (12.2%) in output voltage wave and (3.79%) in load current wave for inductive load. THD in the two stage inverter proposed is (1.8%) in output voltage wave and (0.18%) in load current wave for inductive load. Thus, filter is unnecessary in the two stage inverter. Simulation and experimental results show the effectiveness of the system proposed.

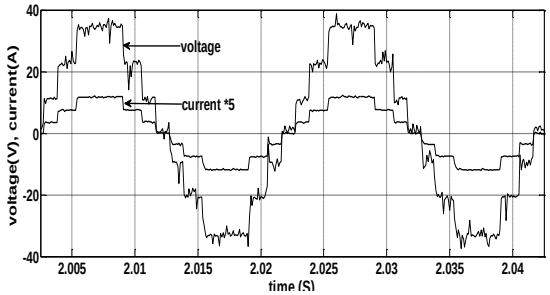


Fig. 23 Experimented output voltage with load current for resistive load

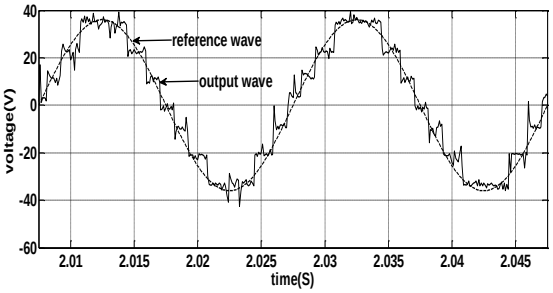


Fig. 24 experimented output voltage for inductive load

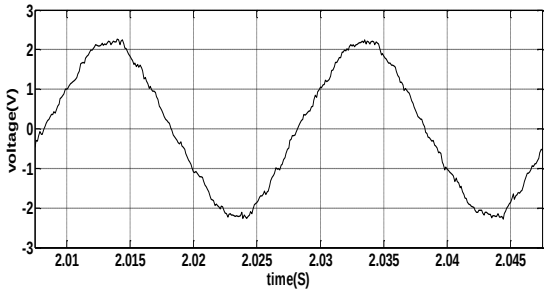


Fig. 25 experimented load current for inductive load

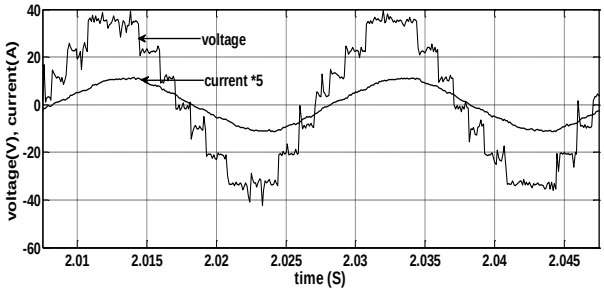


Fig. 26 Experimented output voltage with load current for inductive load

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